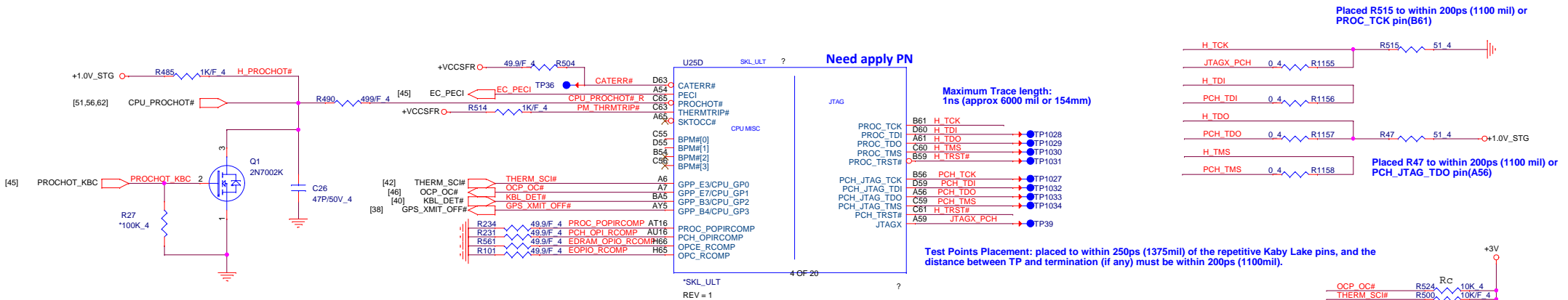
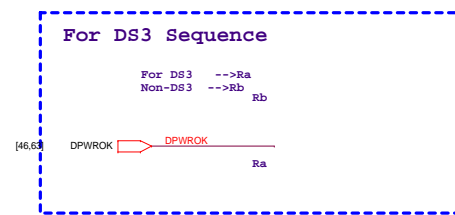
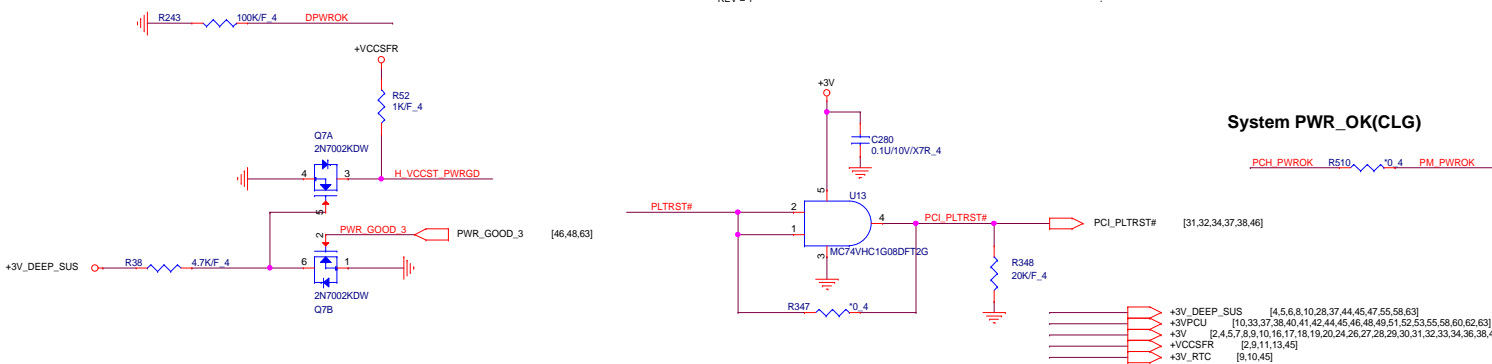
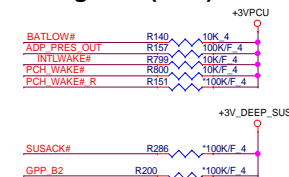
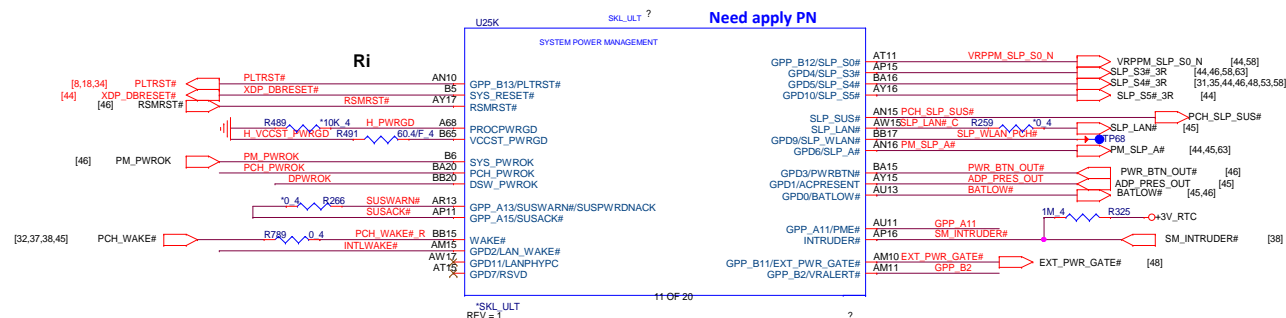
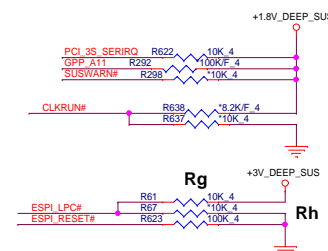
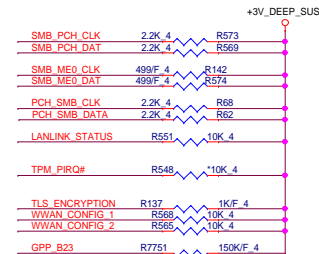


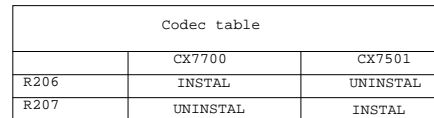
<https://t.me/biosarchive>
<https://t.me/schematics4laptop>





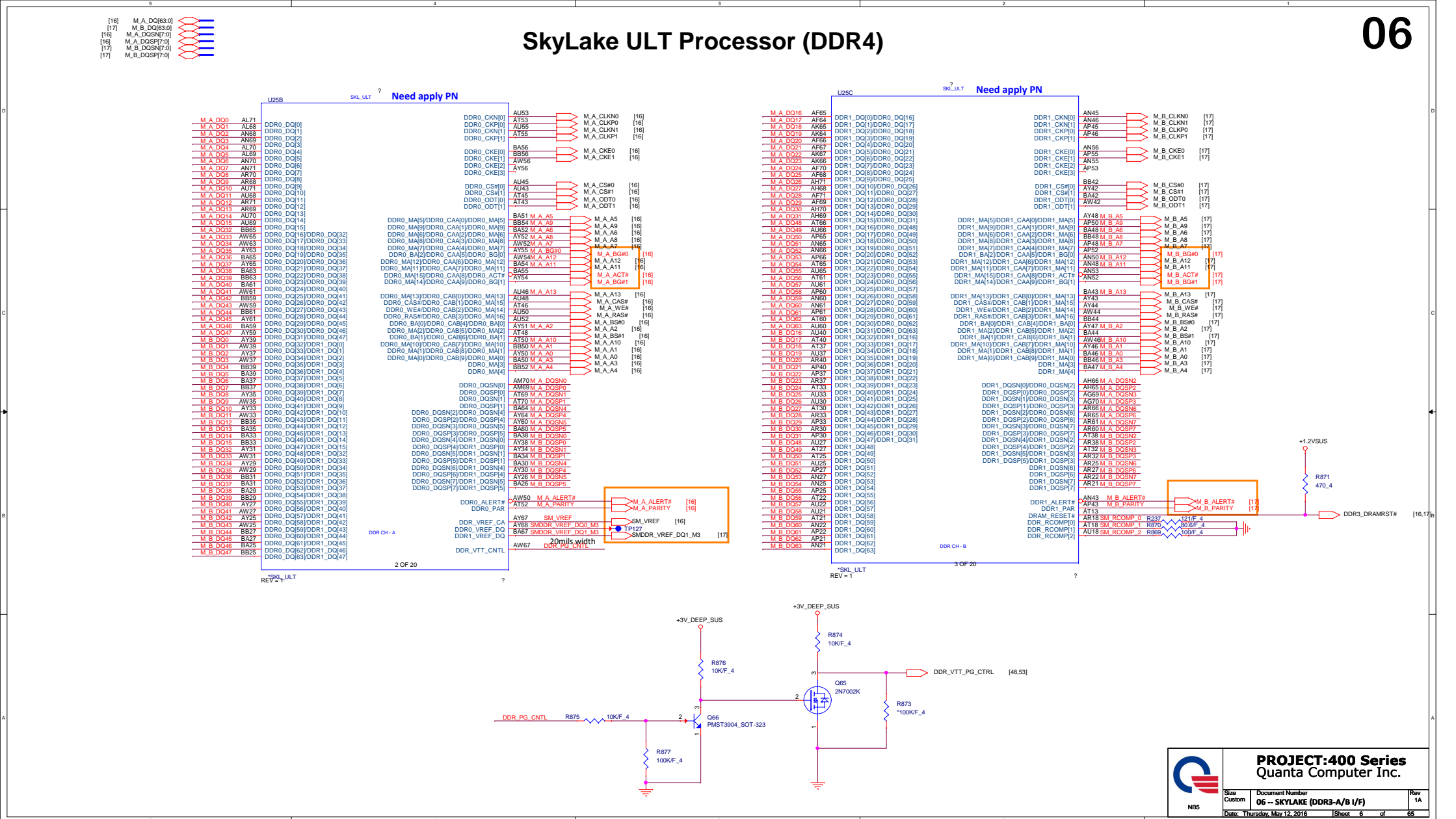
<https://t.me/biosarchive>
<https://t.me/schematics4laptop>



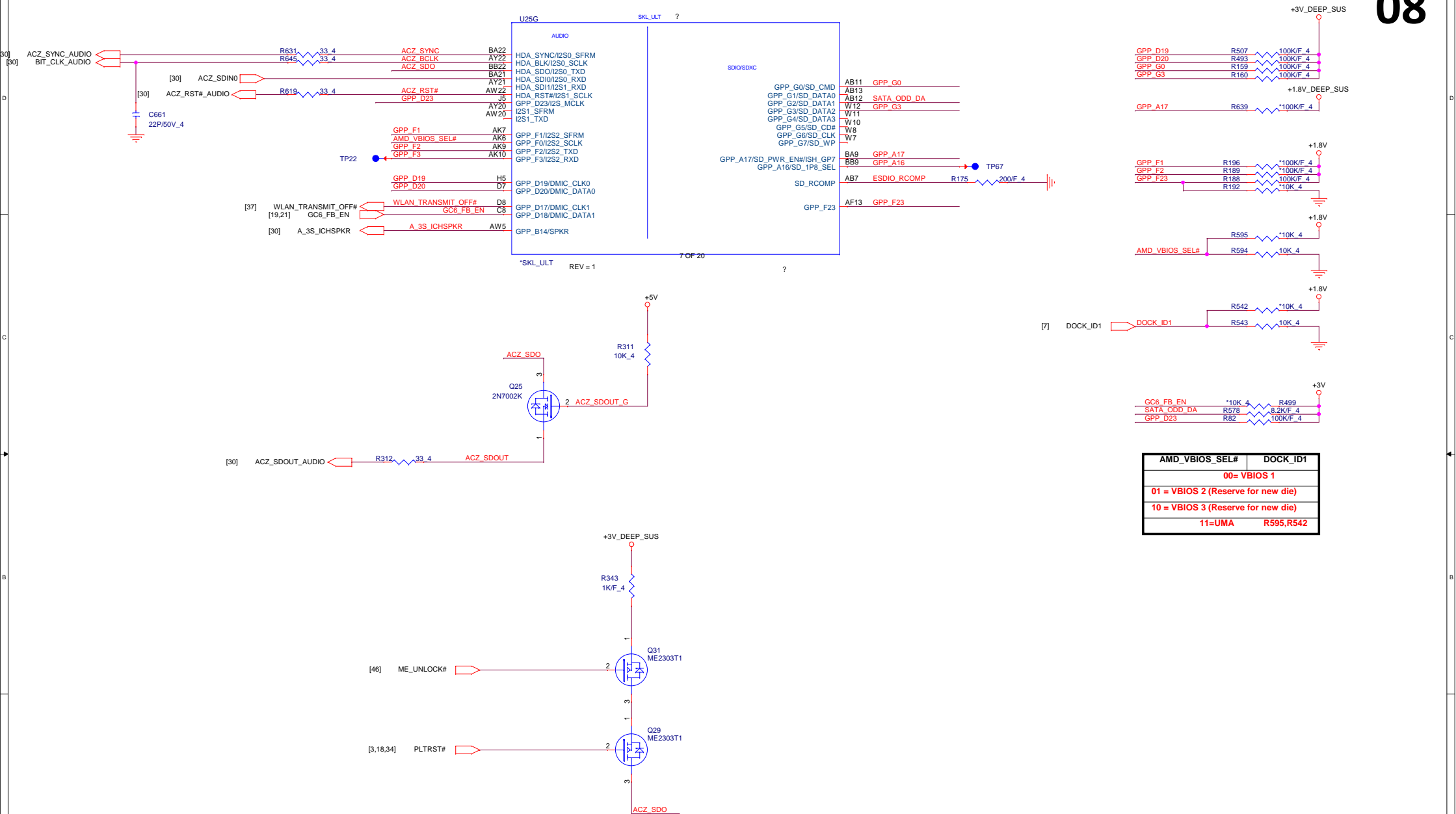


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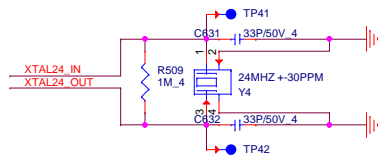
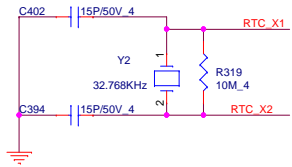
SkyLake ULT Processor (DDR4)



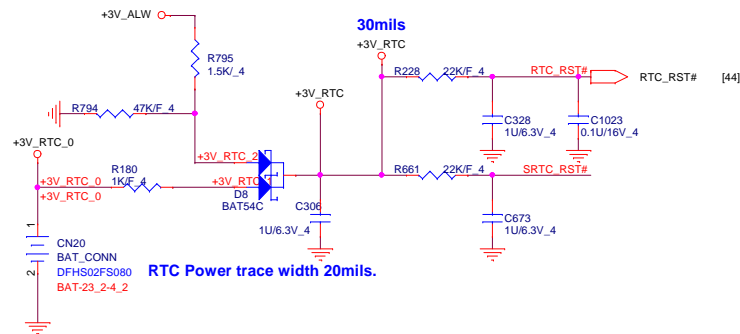




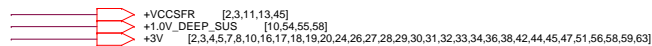
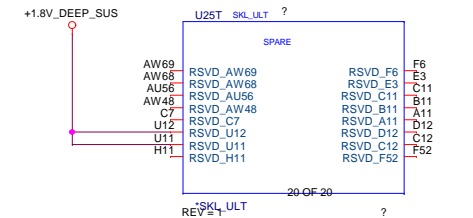
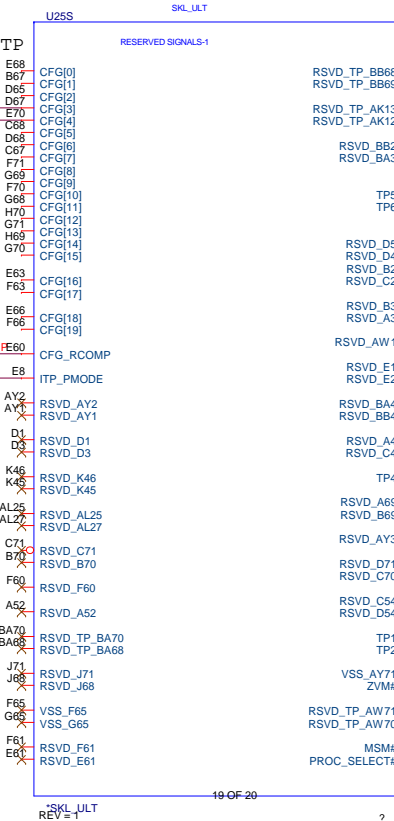
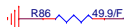
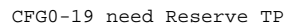
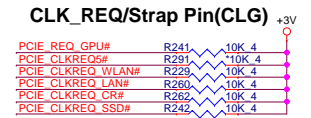
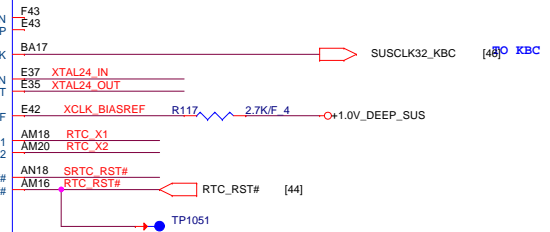
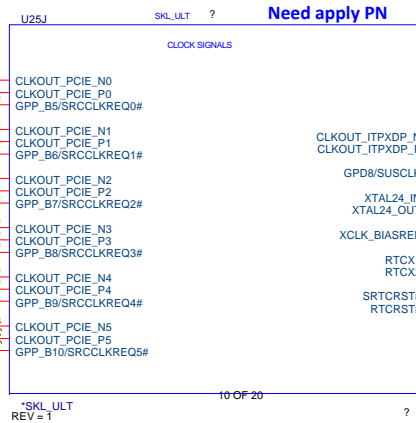
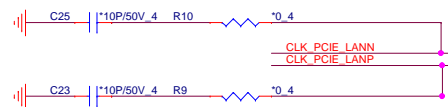
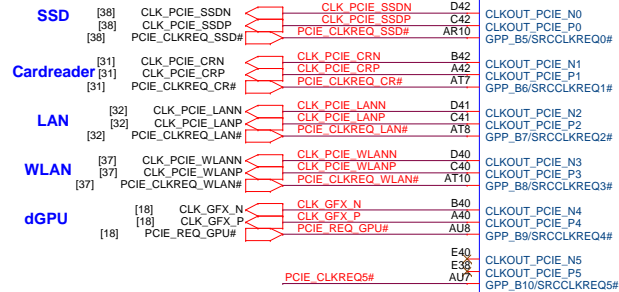
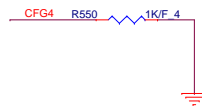
RTC Clock 32.768KHz

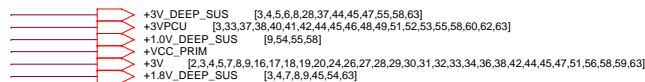
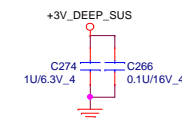
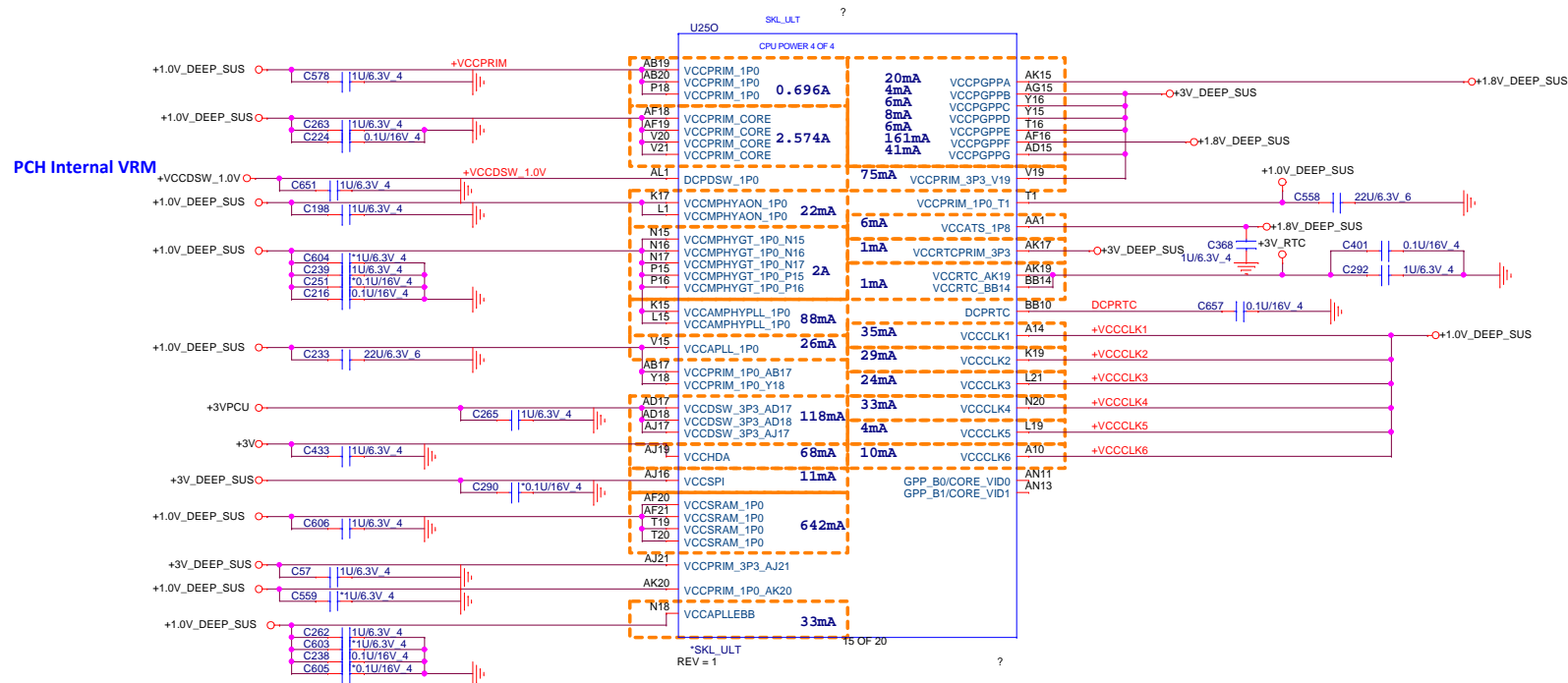


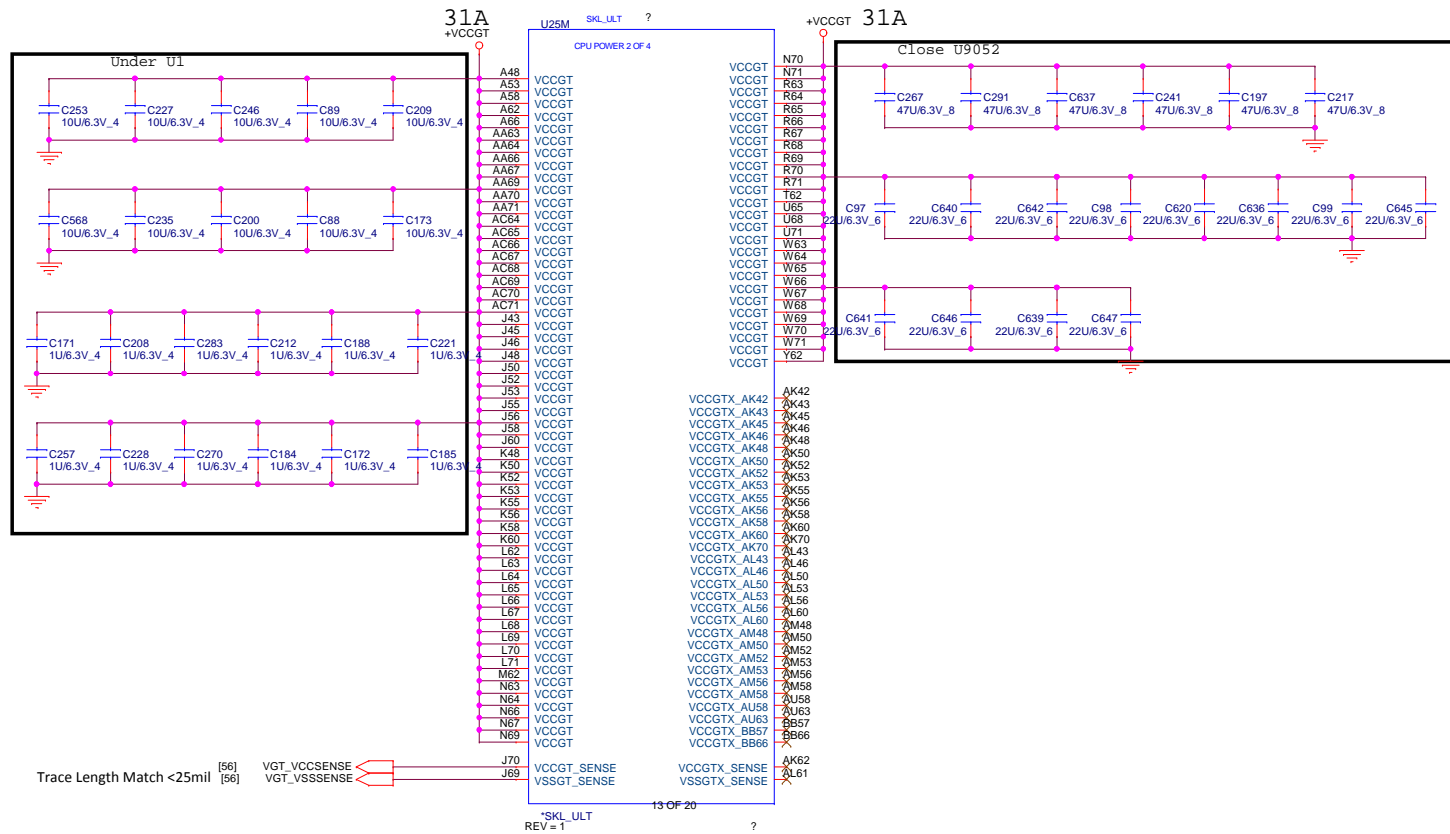
RTC Circuitry(RTC)



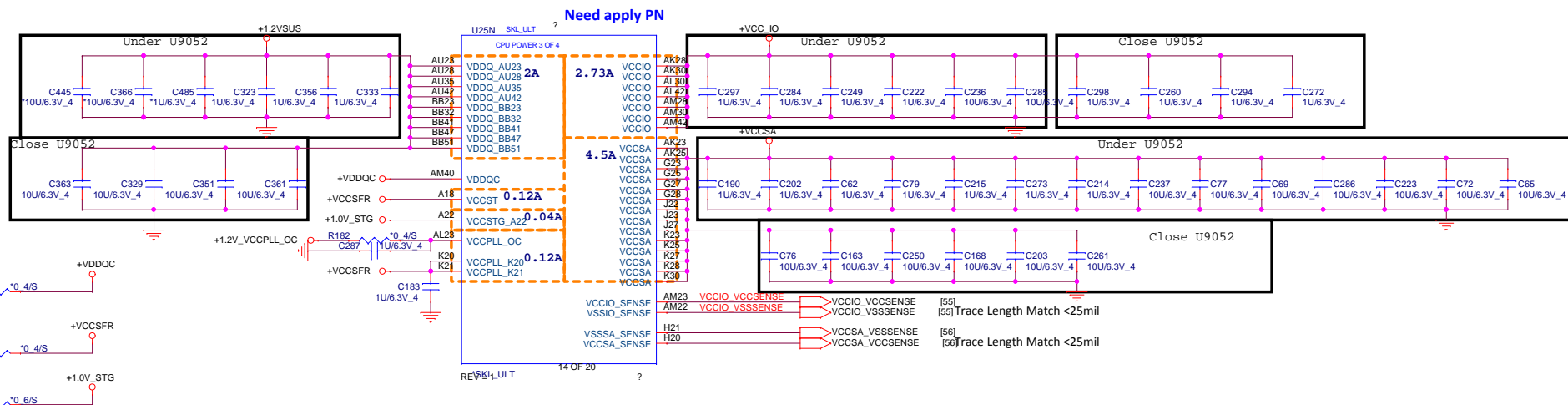
RTC Power trace width 20mils.








Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed




Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CC_EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



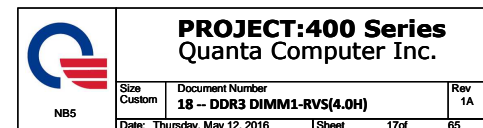
PROJECT:400 Series
Quanta Computer Inc.

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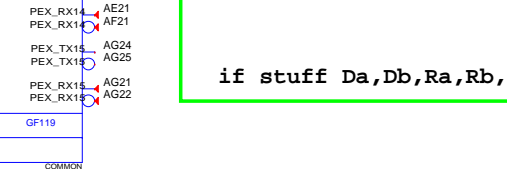
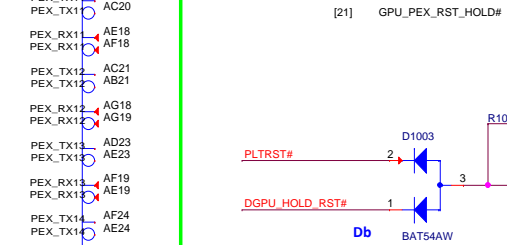
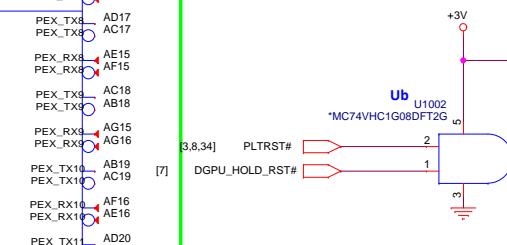
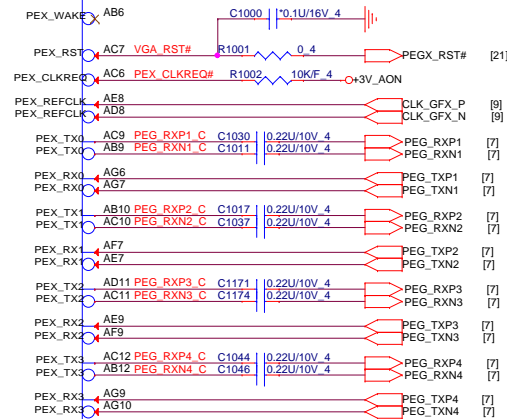
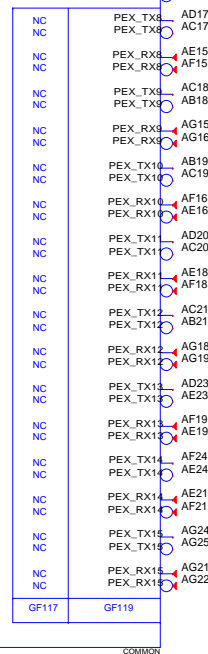
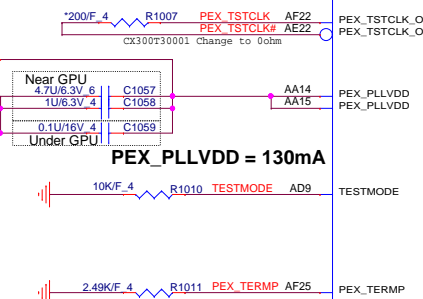
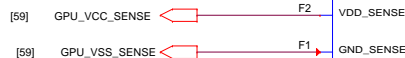
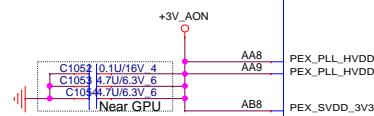
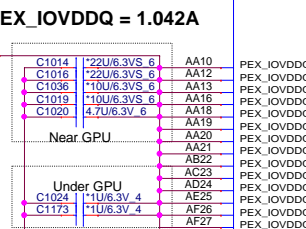
 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size	Document Number	Rev
	15 – HSW XDP & APS		1A
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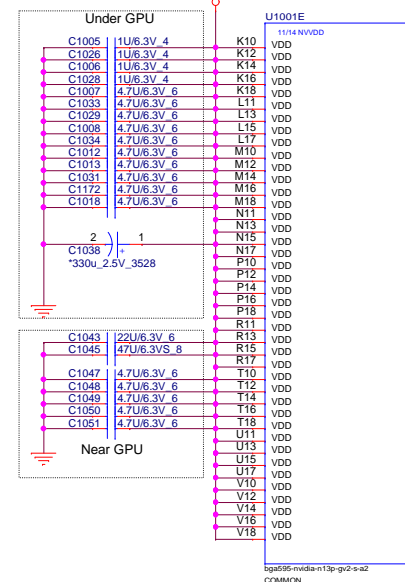


PEX_IOVDD + PEX_IOVDDQ = 1.042A

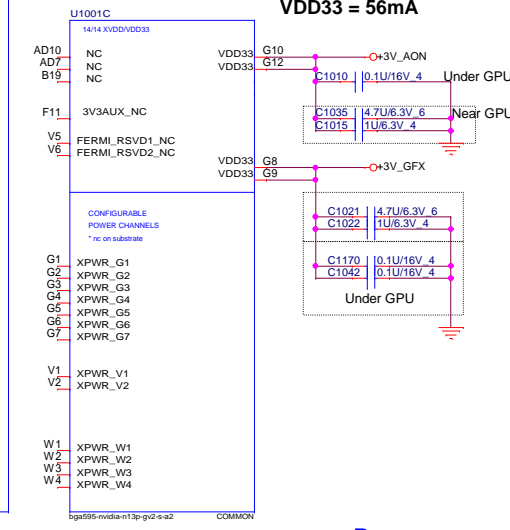
PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA



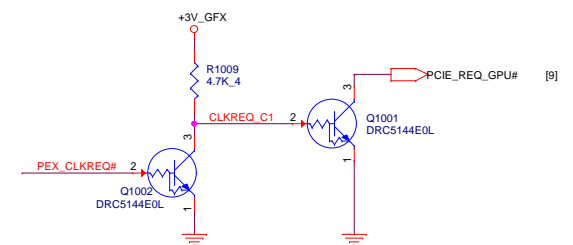
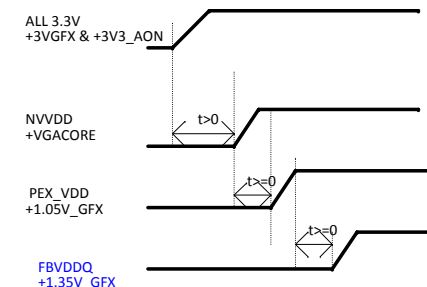
NVDD = 32.22 ~ 26.66 A +VGACORE



VDD33 = 56mA



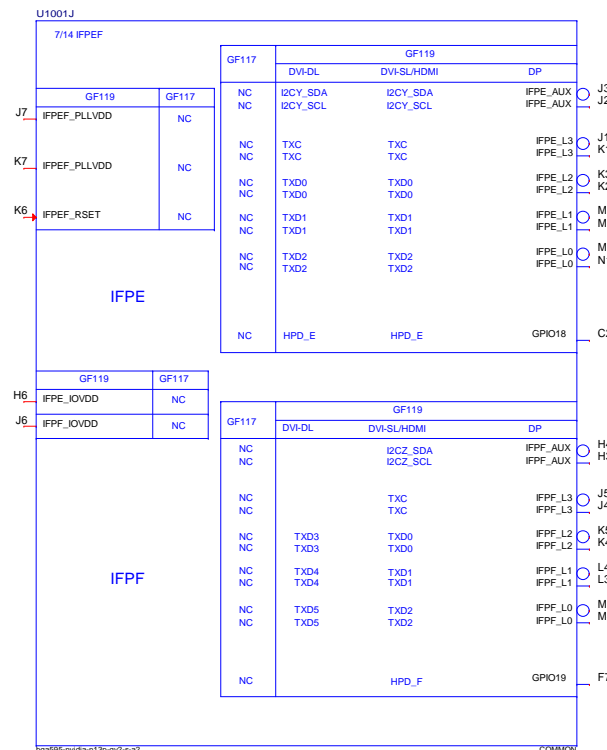
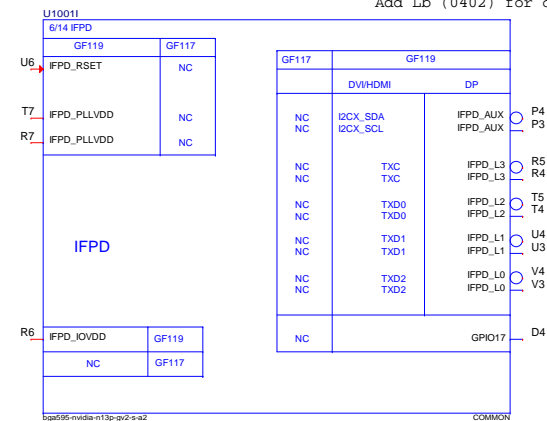
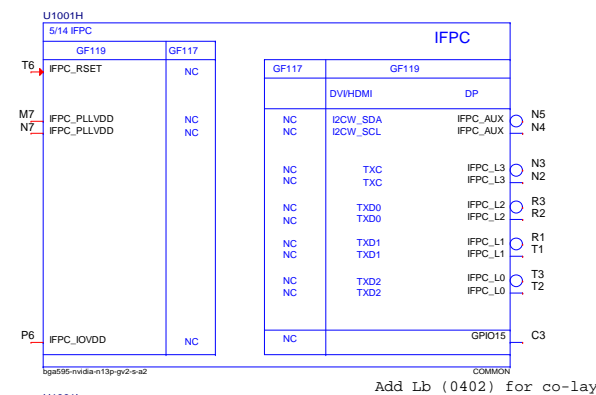
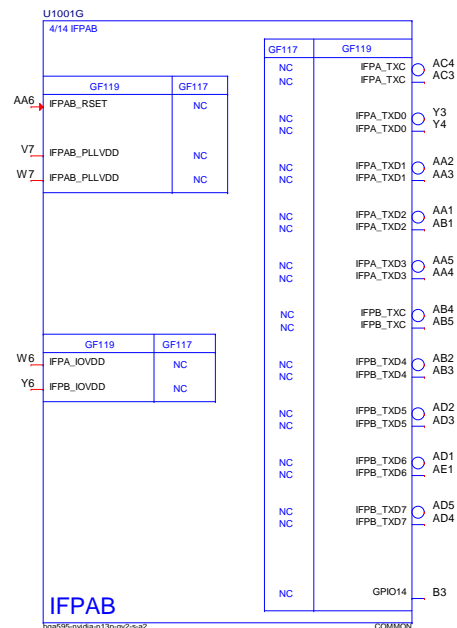
Power up sequence



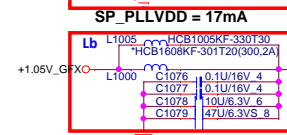
if stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd

	PROJECT:400 Series Quanta Computer Inc.	
	Size Custom Date: Thursday, May 12, 2016	Document Number N16S-GMR (PCIe I/F) /NVDD Sheet 18 of 65

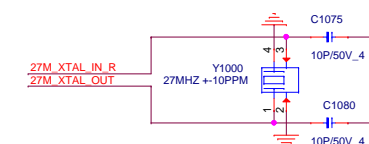
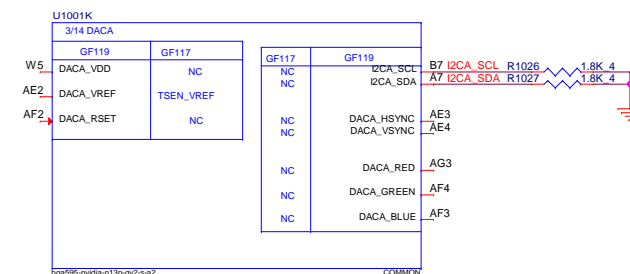
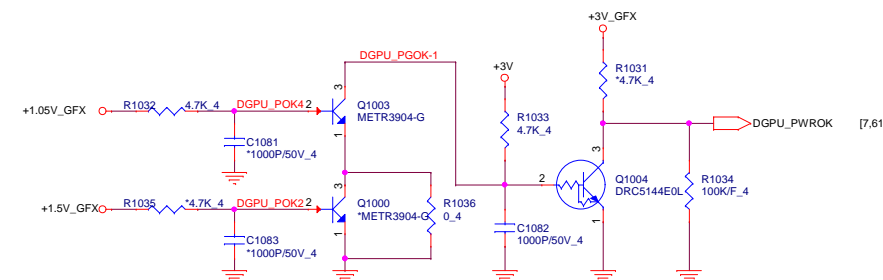


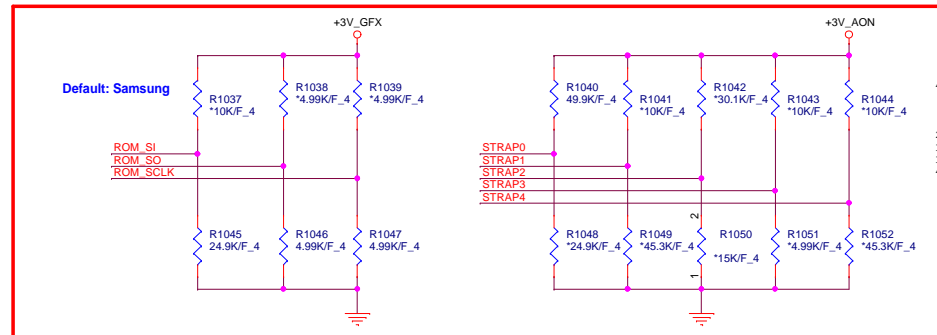
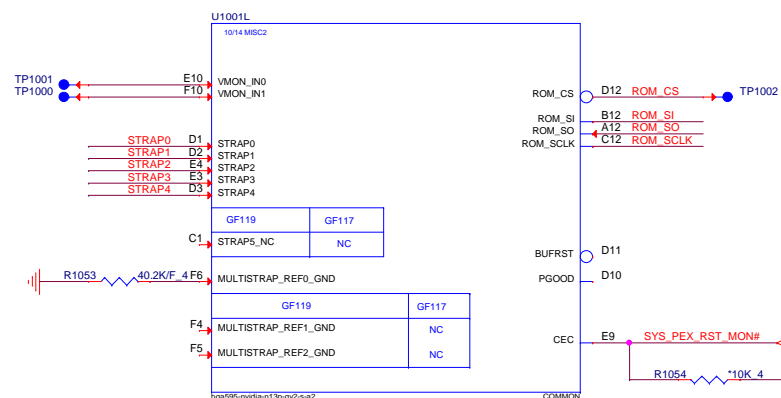


PLLVD = 38mA Add La (0402) for co-layer



VID_PLLVDD = 41mA

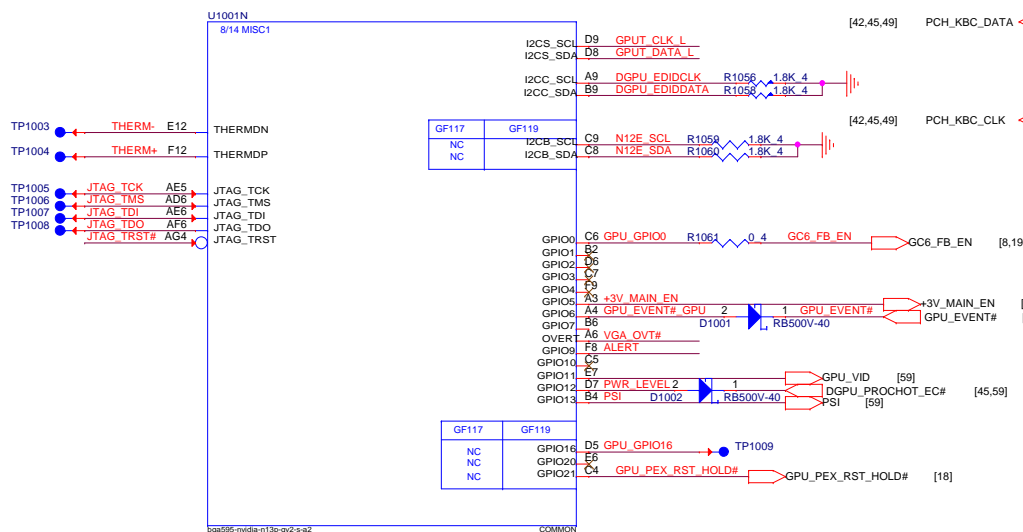




4.99k	CS24992FB26
10k	CS31002FB26
15k	CS31502FB24
20k	CS32002FB29
24.9k	CS32492FB16
30.1k	CS33012FB18
34.8k	CS33482FB06
45.3k	CS34532FB18

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0101	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMMORY_VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



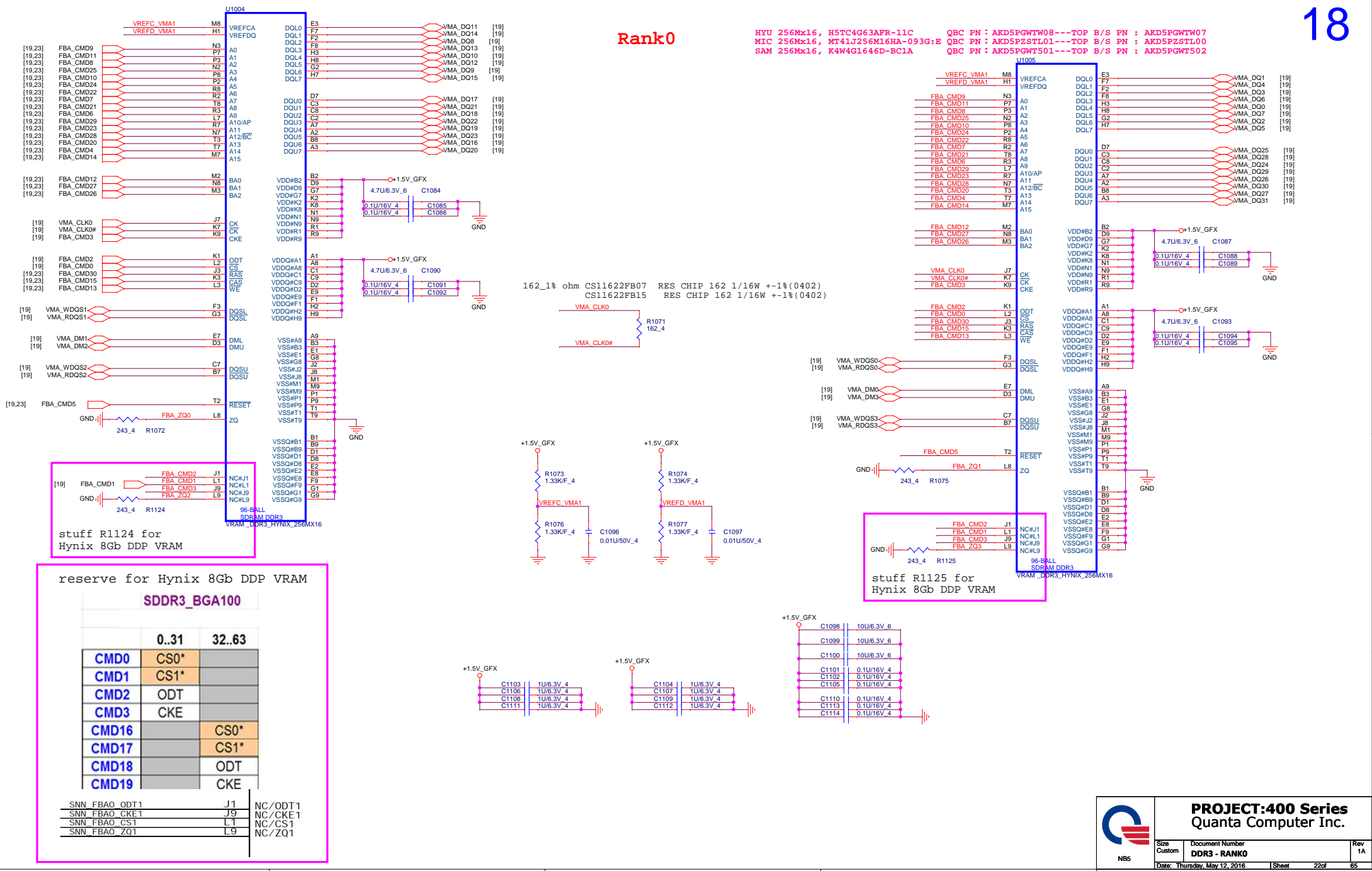
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16S-GMR (GPIO/STRAPS)	1A
Date: Thursday, May 12, 2016	Sheet 21 of 65	

Rank0

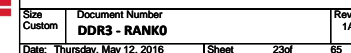
HYU 256Mx16, H5TC4G63APR-11C
 MJC 256Mx16, MT4L1256M16HA-093G:E
 SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
 QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
 QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

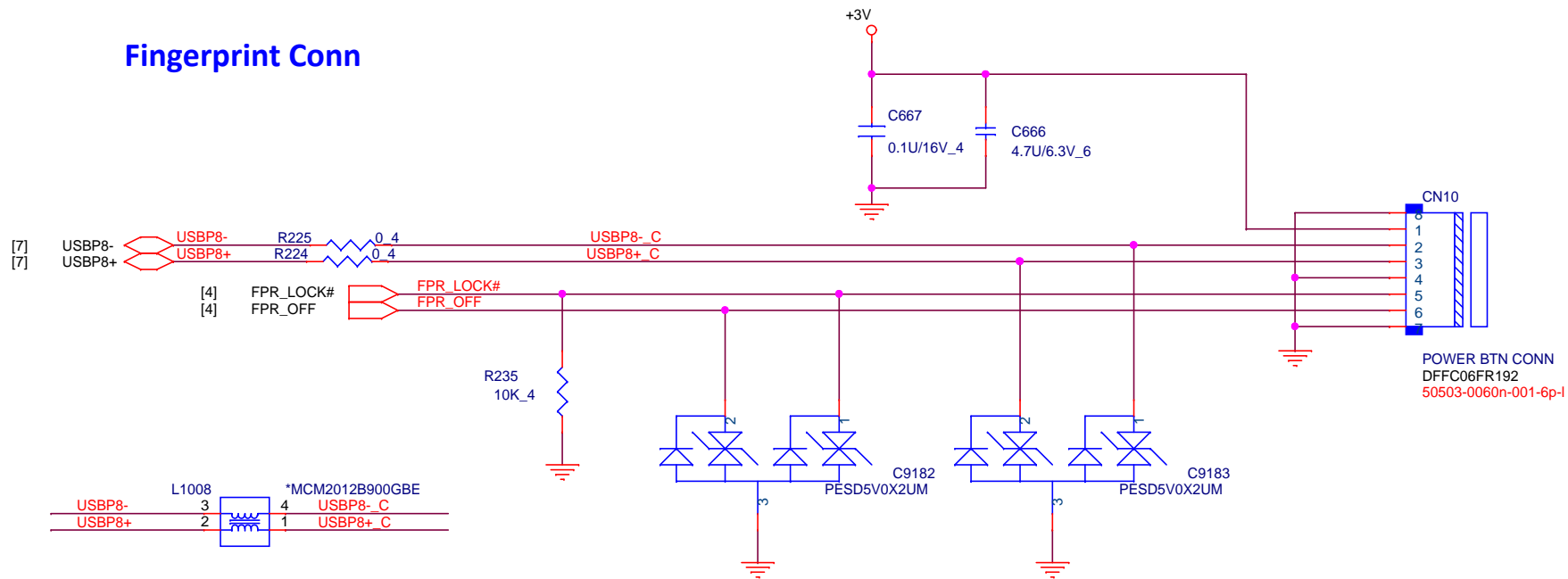


PROJECT:400 Series
Quanta Computer Inc.

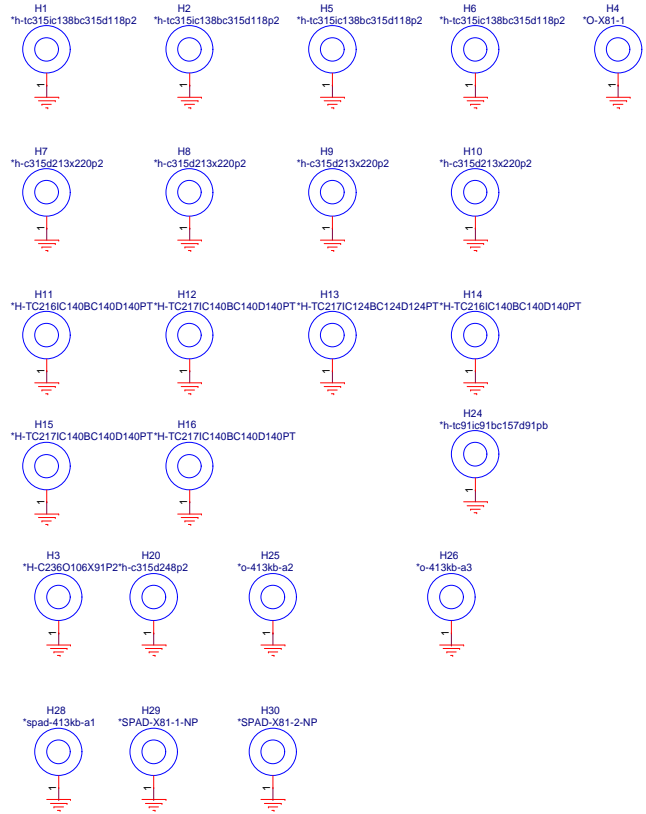
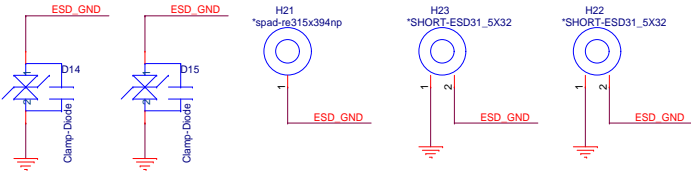
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Custom	DDR3 - RANK0	1A
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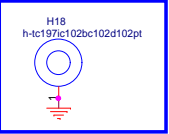
Fingerprint Conn



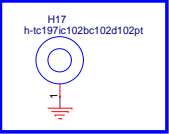
Hole



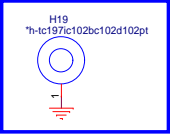
WLAN nut



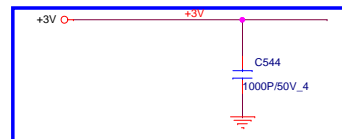
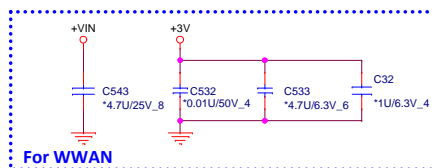
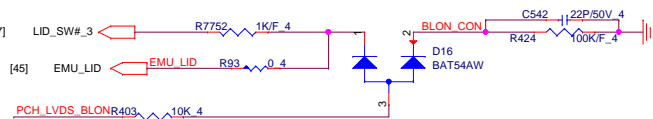
SSD nut



WWAN nut

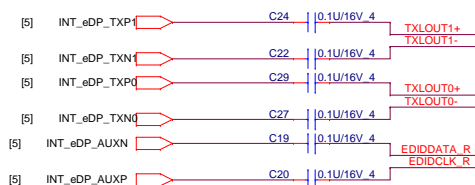
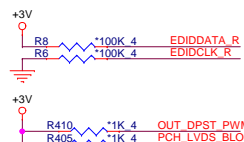
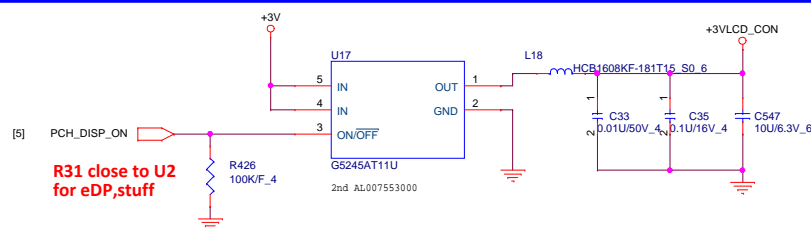


LID Switch

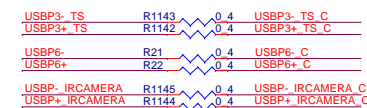
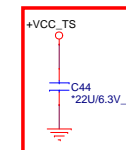


ALF@20151019:

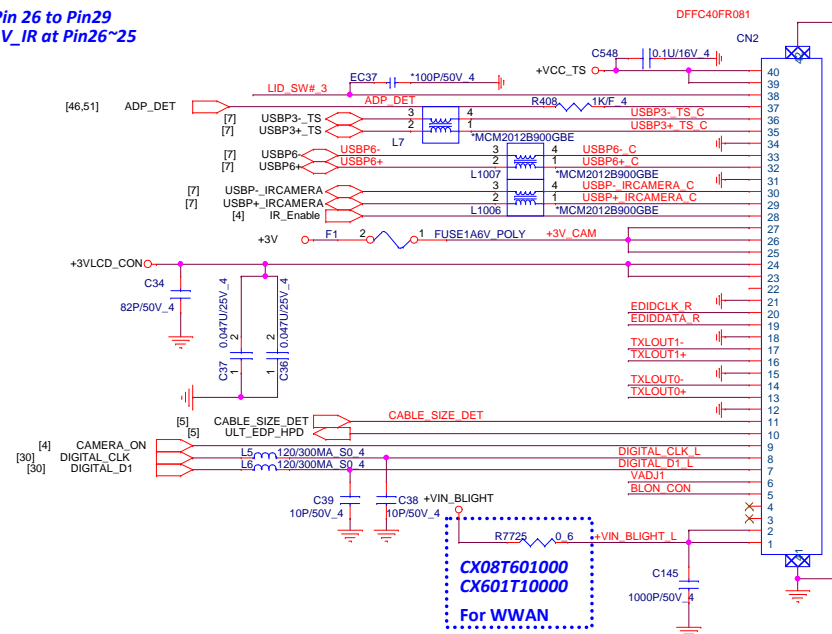
1. Designed Reserve 4Pins for IR CCD Pin 26 to Pin29
2. Combined the +3V & +3V CAM & +3V IR at Pin26~25

**LVDS Conn.**

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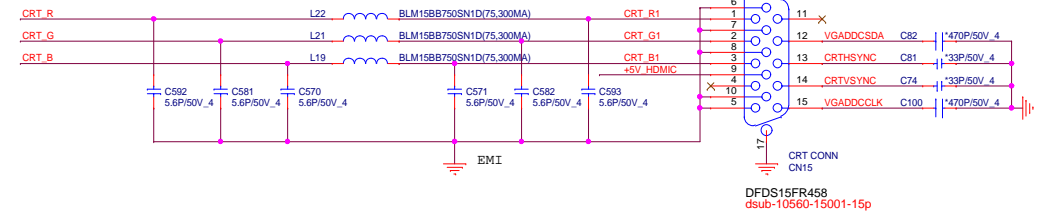
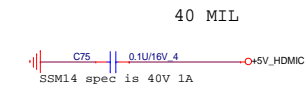
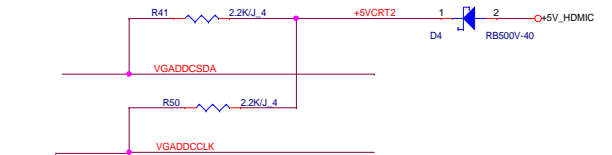
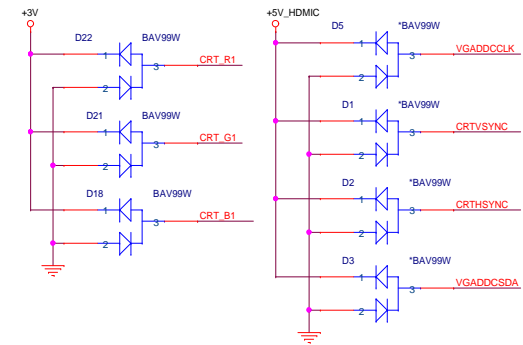
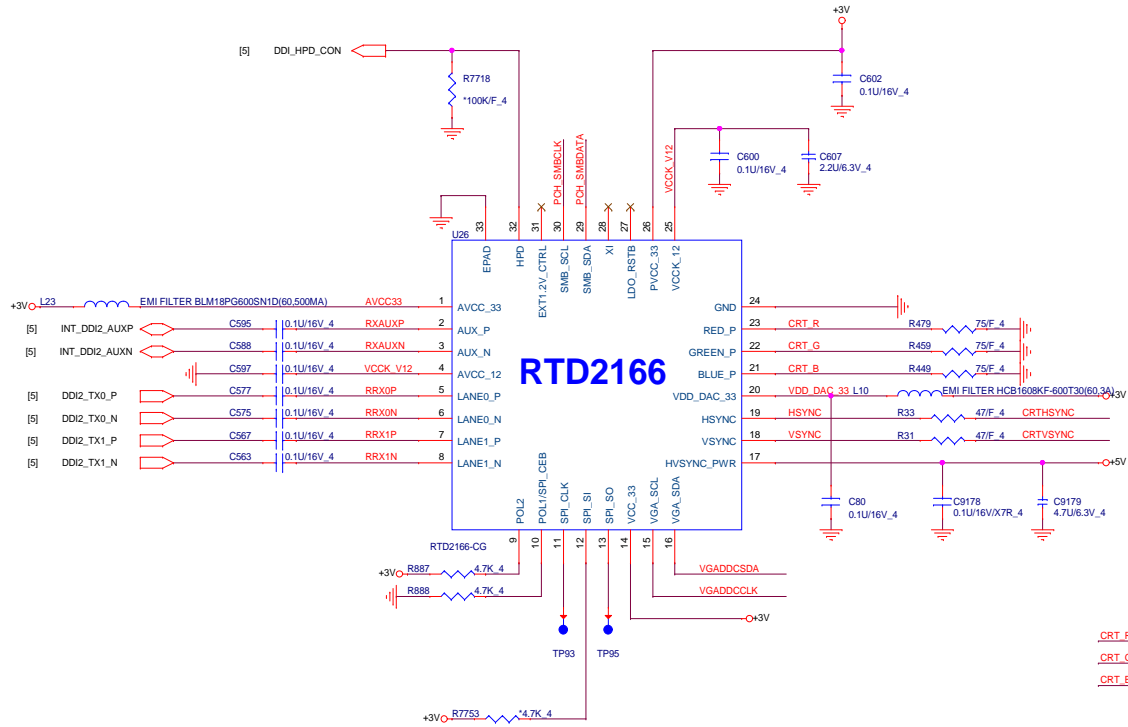


GS12401-1011-9H
lvds-50671-04041-001-40p-



PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 26 -- LCD CONN/LID/CAM/D-MIC	Rev 1A
Date: Thursday, May 12, 2016	Sheet 26 of 65	



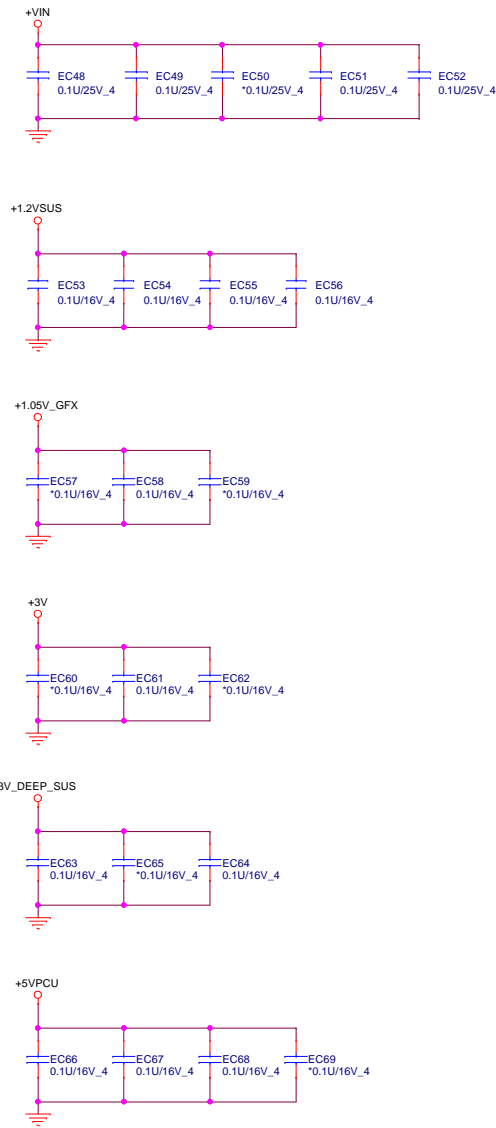
CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
 ROM or EEPROM mode: connect to PCH SMBUS
 IIC Protocol is used

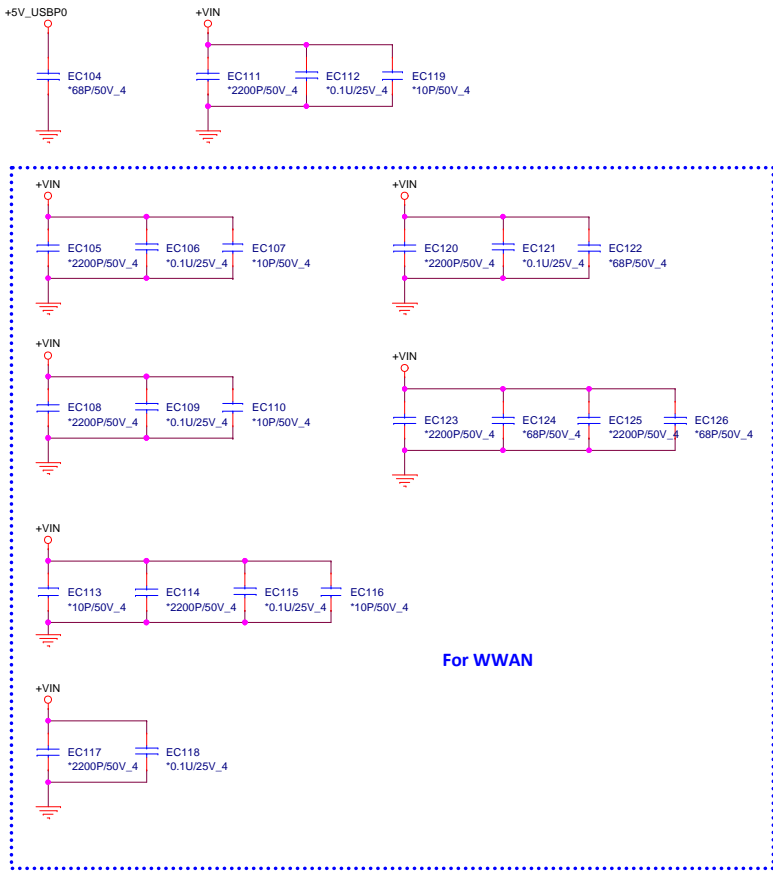
RTD2168 Slave Address:
 0x64/0x65 and 0x68/0x69



EMI CAP

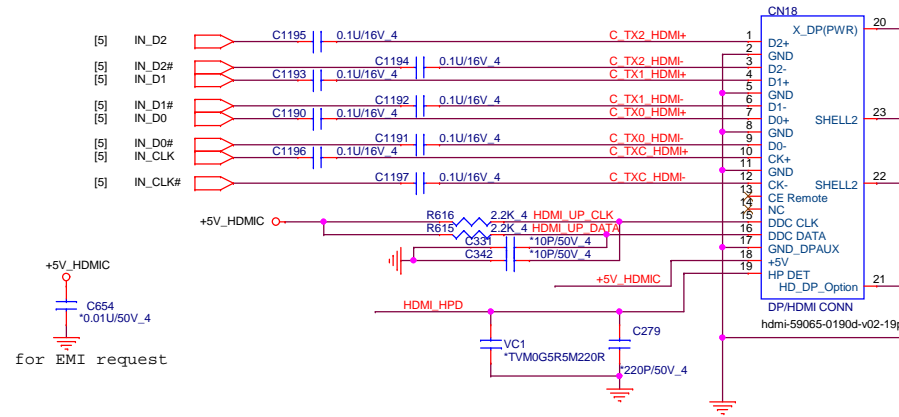
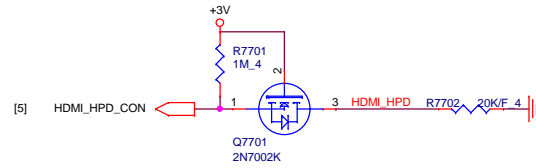


RF Cap



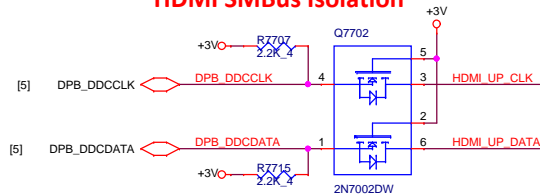
EMI Solution

C_TX2_HDMI+	R208	120/F 4	C_TX2_HDMI-
C_TX1_HDMI+	R194	120/F 4	C_TX1_HDMI-
C_TX0_HDMI+	R178	120/F 4	C_TX0_HDMI-
C_TXC_HDMI+	R221	120/F 4	C_TXC_HDMI-

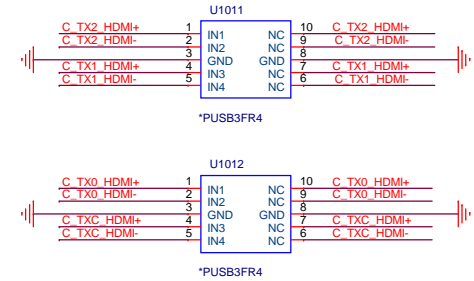
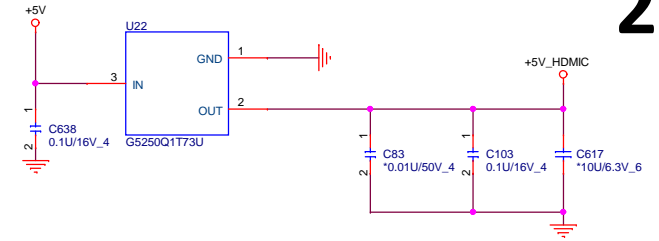
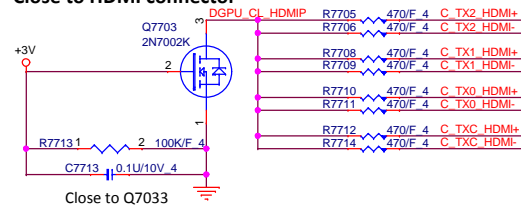


for EMI request

HDMI SMBus Isolation

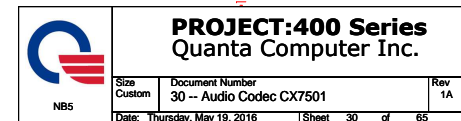


Close to HDMI connector

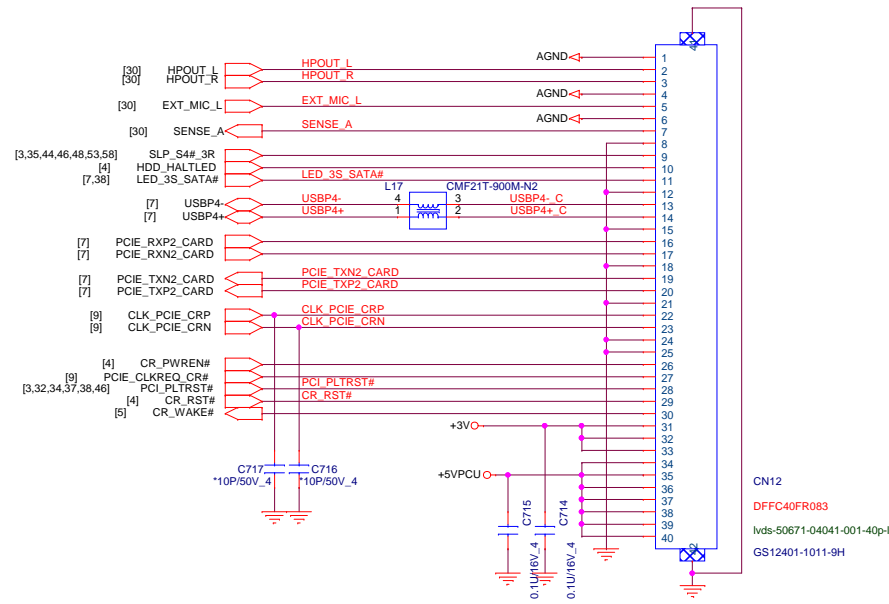


PROJECT:400 Series
Quanta Computer Inc.

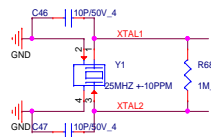
Size Custom	Document Number 29 -- HDMI CONNECTOR	Rev 1A
Date: Thursday, May 12, 2016	Sheet 29 of 65	



USB/Card Reader/Headphone_Mic Combo Jack Daugther Board Connector



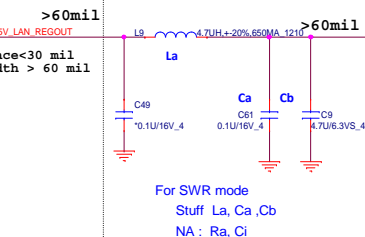
LAN & RJ45



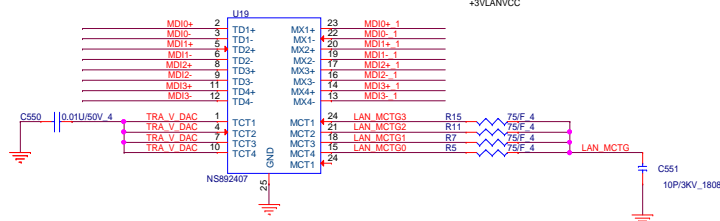
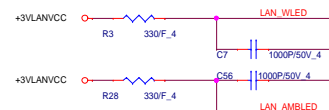
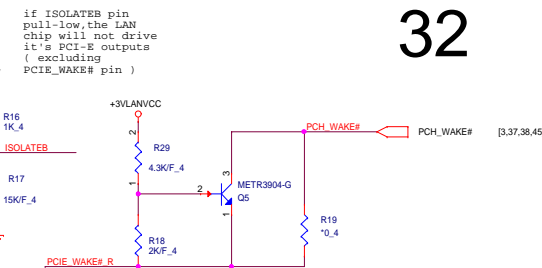
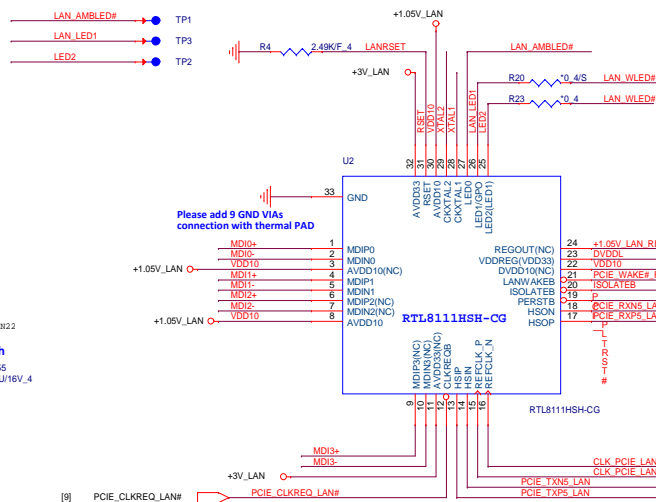
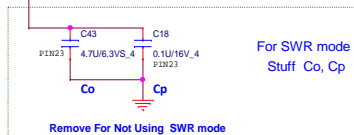
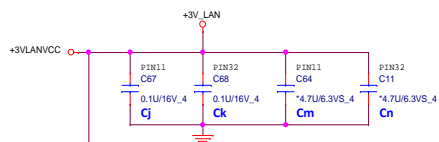
Power trace Layout 寬度> 60mil

* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8, 30

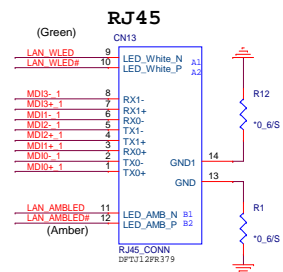
* Place Cg,Ch
close to each VDD10 pin-- 22(reserved)



- * Place Cj and Ck, close to each VDD33 pin-- 11, 32
- * For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



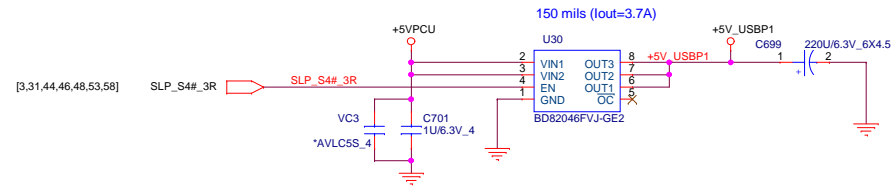
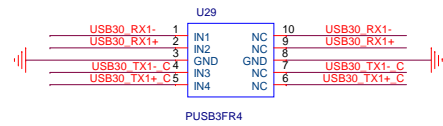
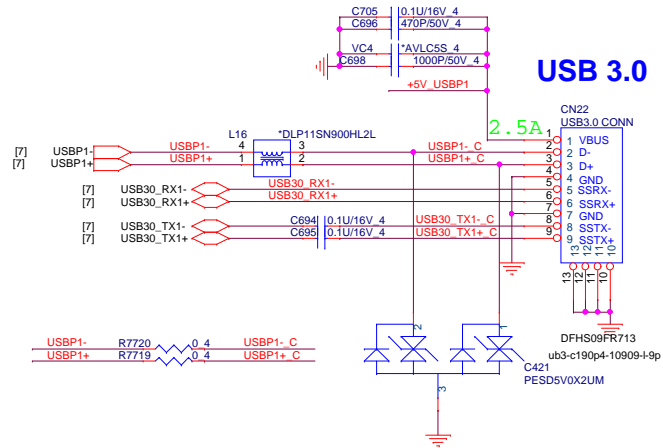
For GiGA BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,33,34,36,38,42,44,45,47,51,56,58,59,63]

[58] +3V
+3VLAVCC

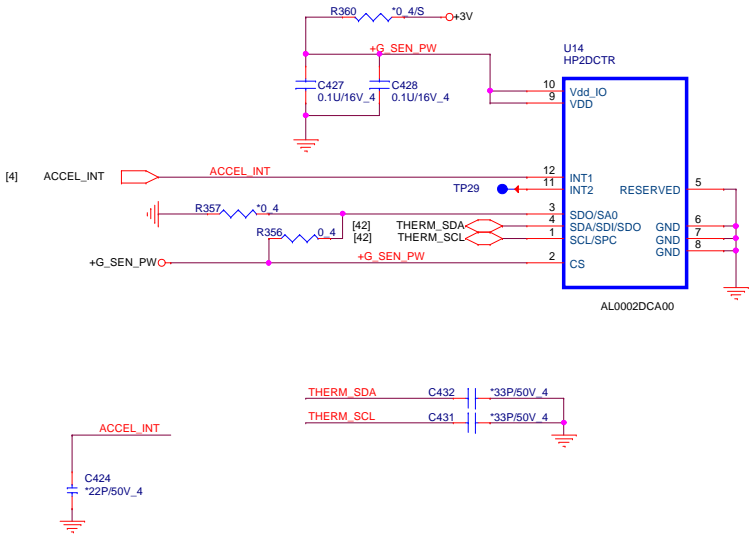




[28,31,44,49,50,51,52,53,54,56,57,58,59,60,61,63] +5VPCU

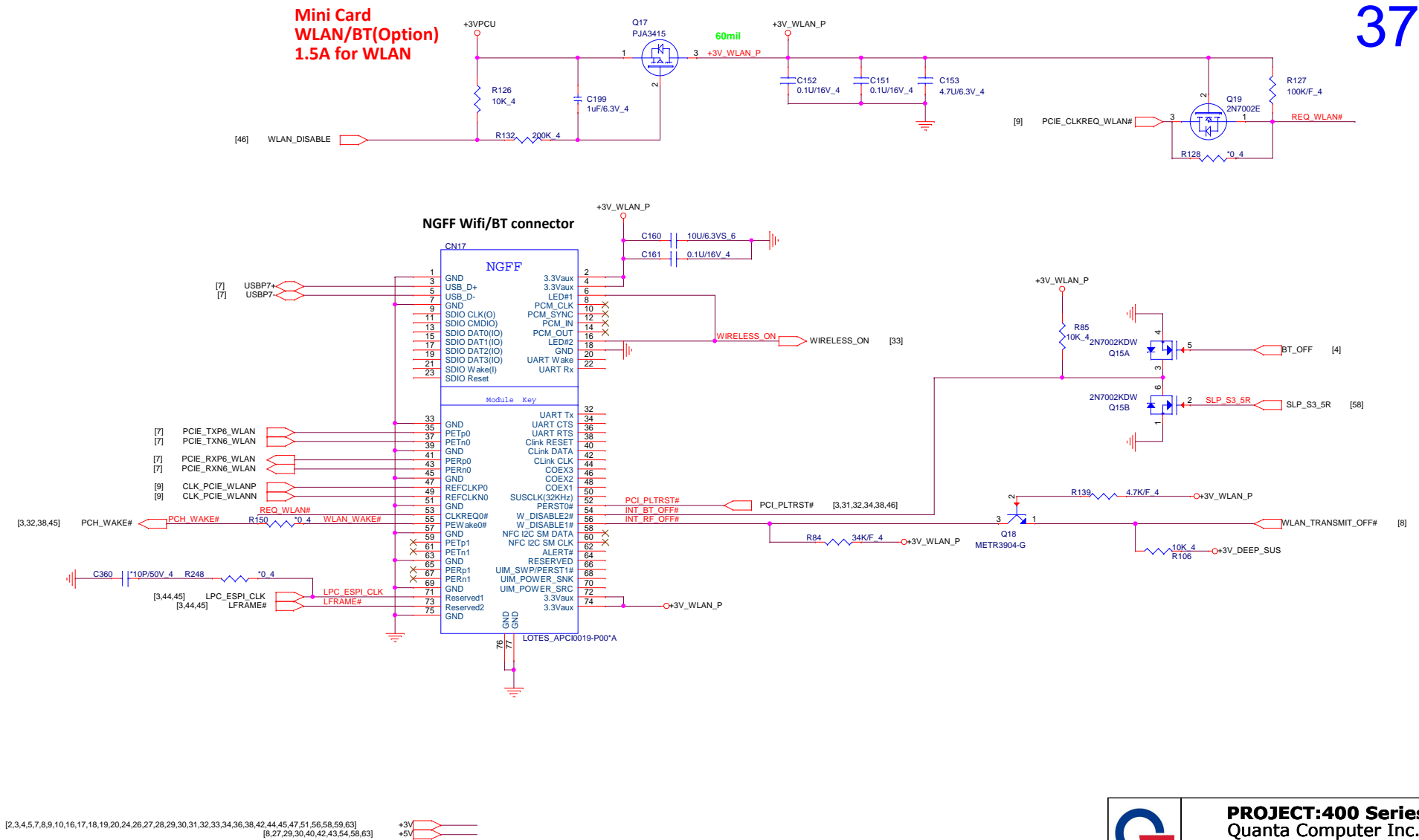
[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +3VPCU

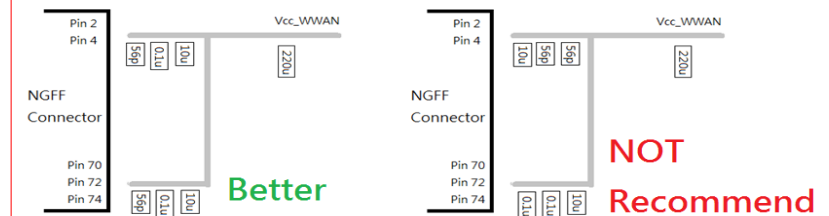
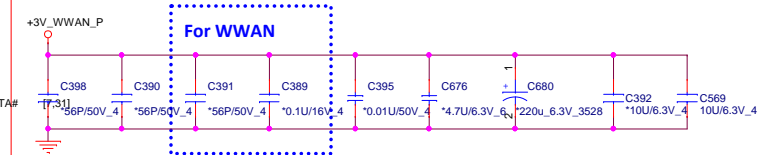
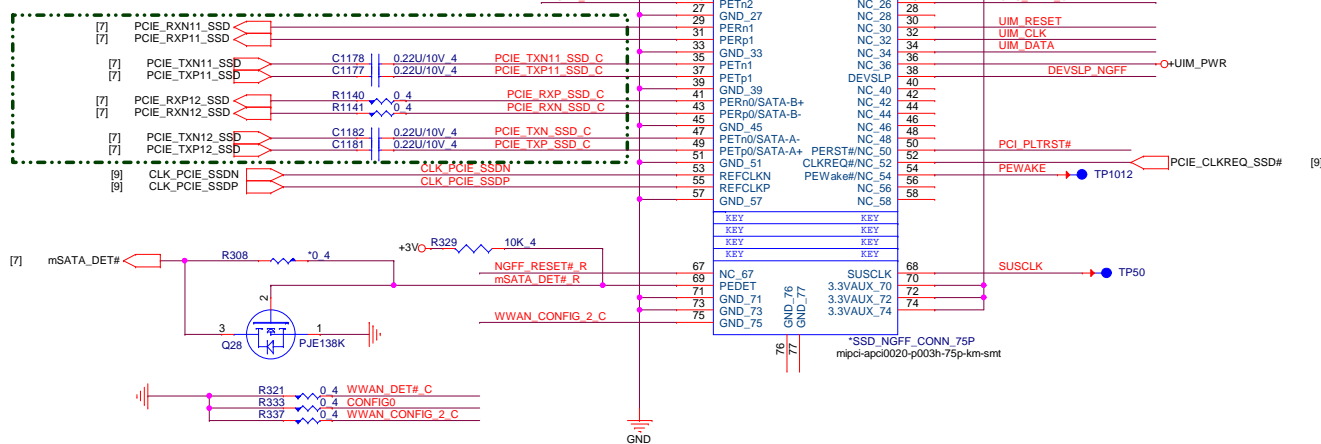
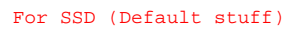
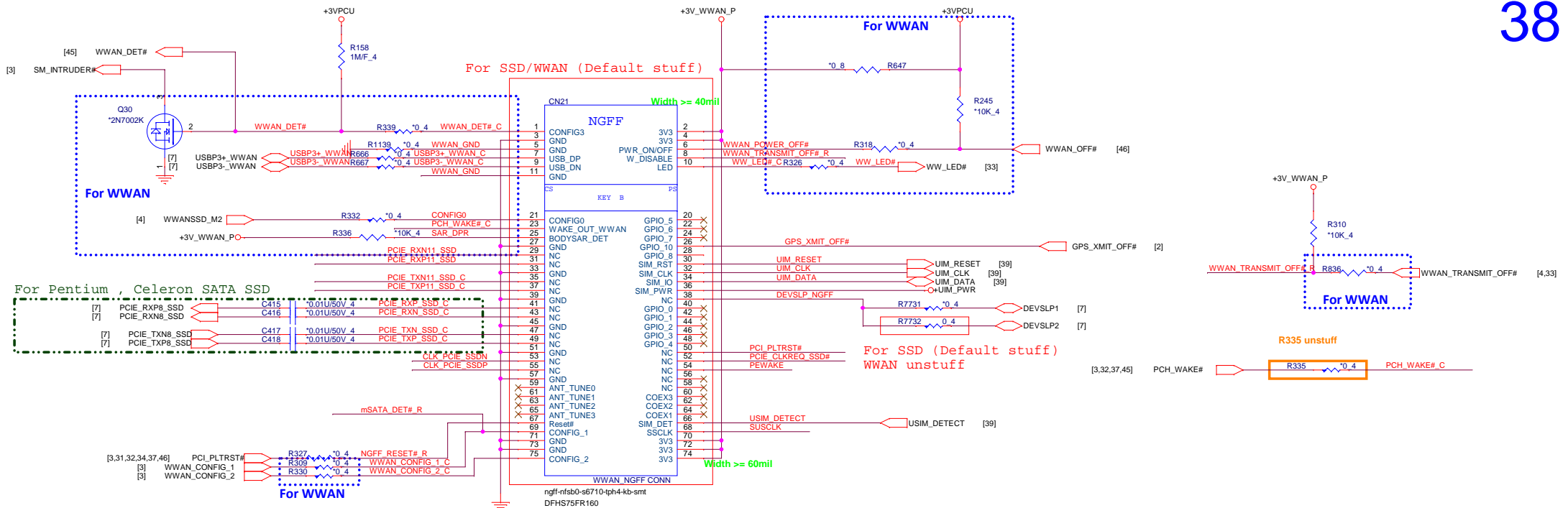
Accelerometer Sensor



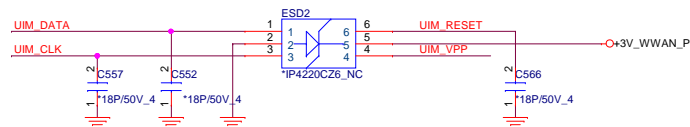
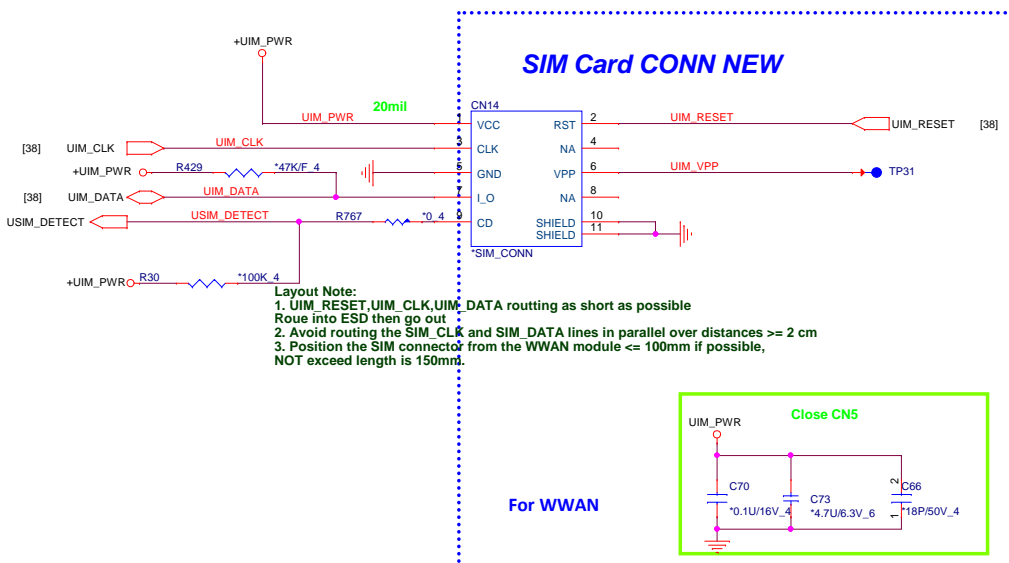
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,38,42,44,45,47,51,56,58,59,63] +3V

[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +3VPCU





+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

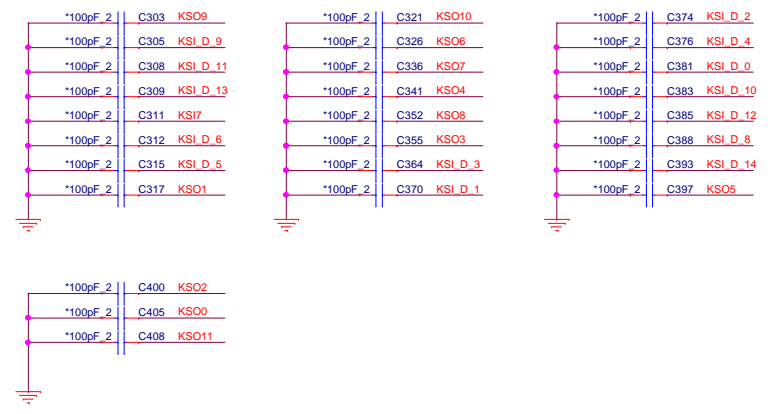
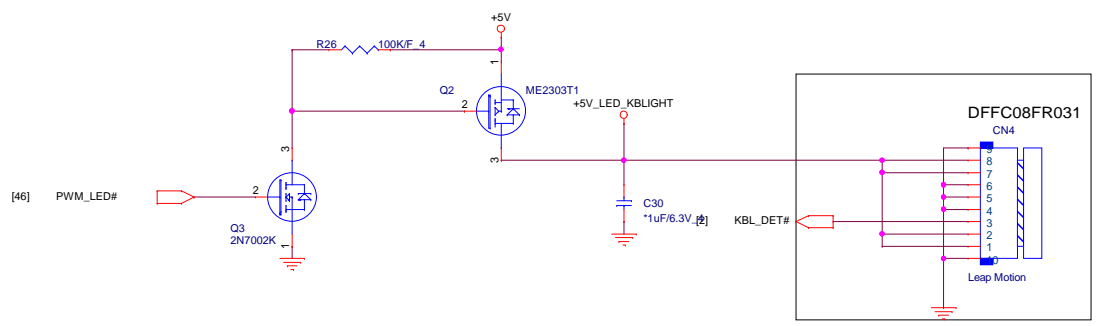
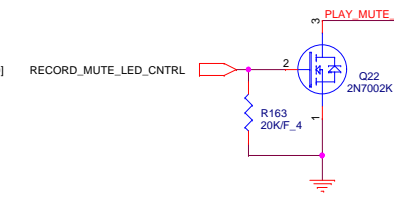
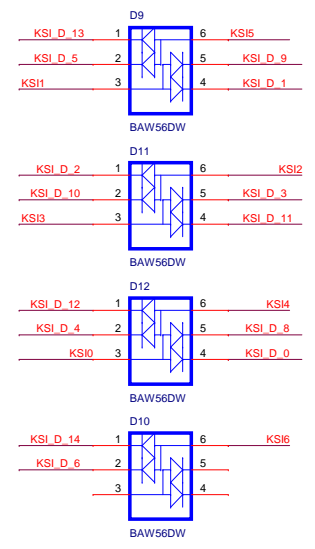
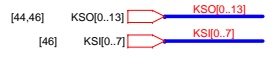
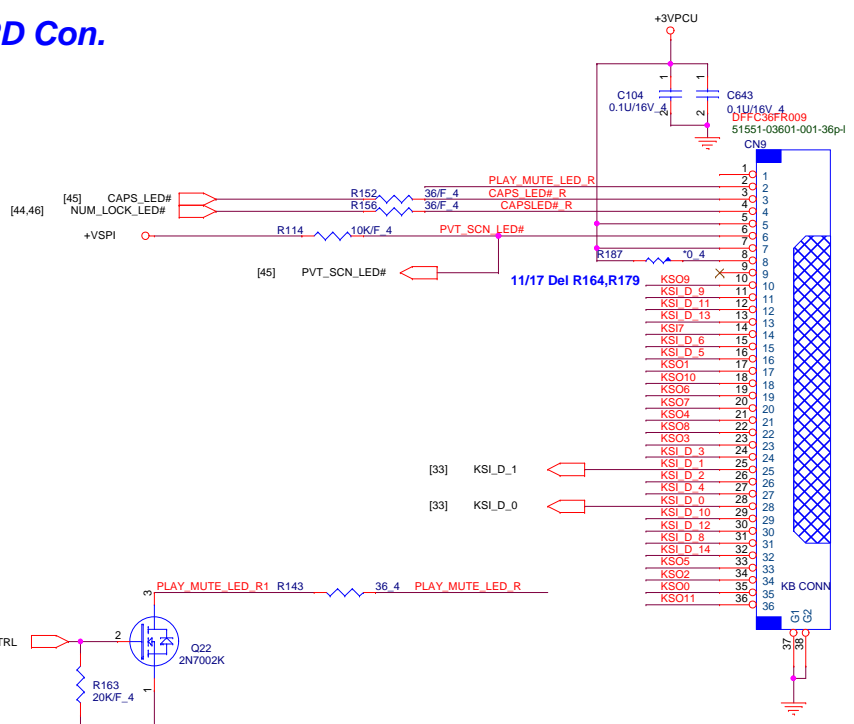


Trace Length and Routing

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.↵
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.↵
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.↵
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.↵

SIM Power^{4J}

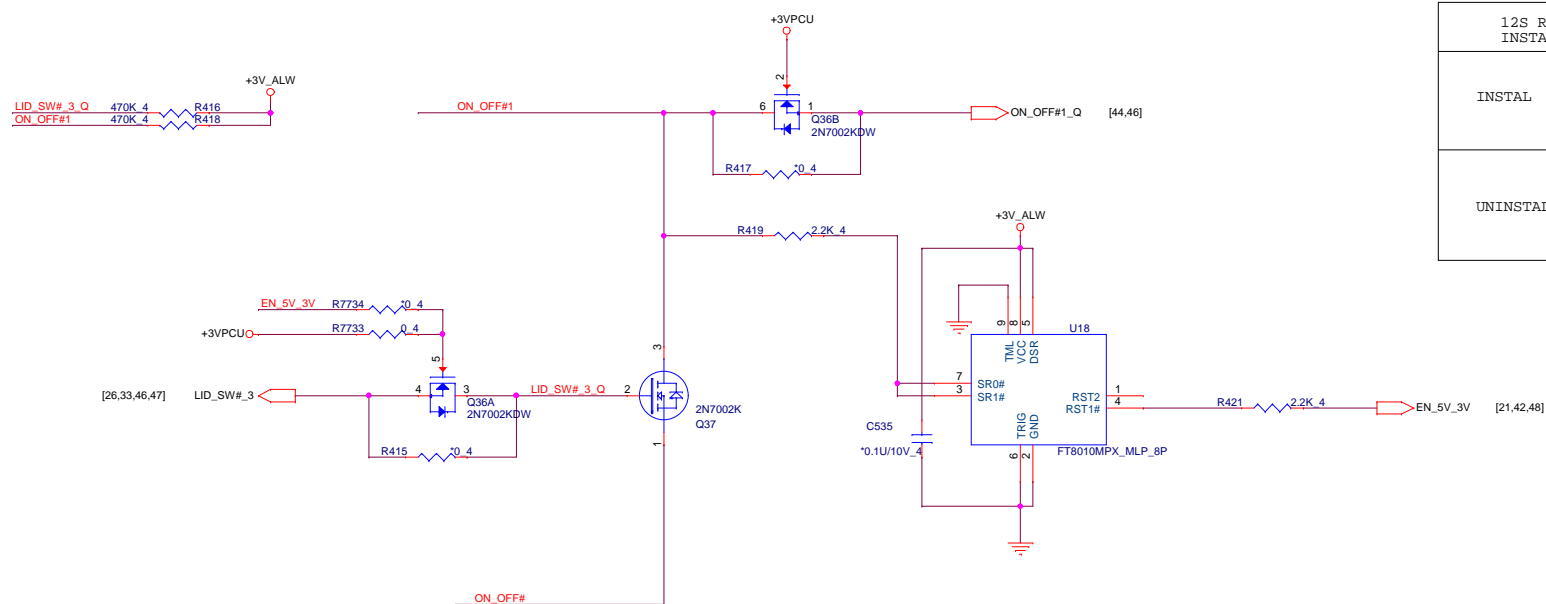
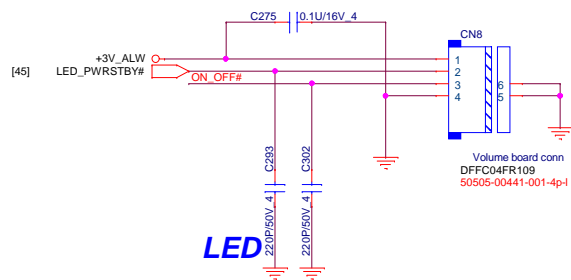
- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.⁴⁾
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.⁴⁾



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
[8,27,29,30,42,43,54,58,63]

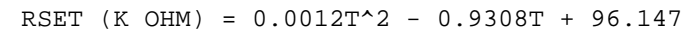


Power Botton Connector

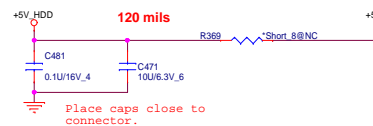
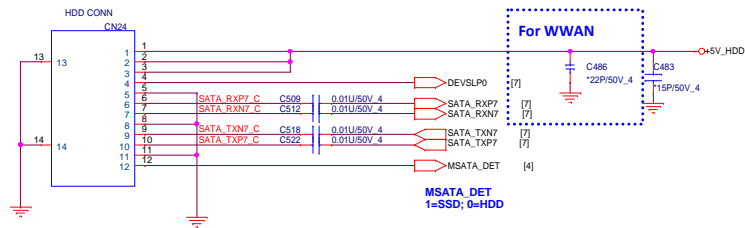


12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R10703 R581 R595
UNINSTAL	R10754 Q7080	R10755 Q7081





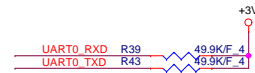
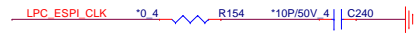
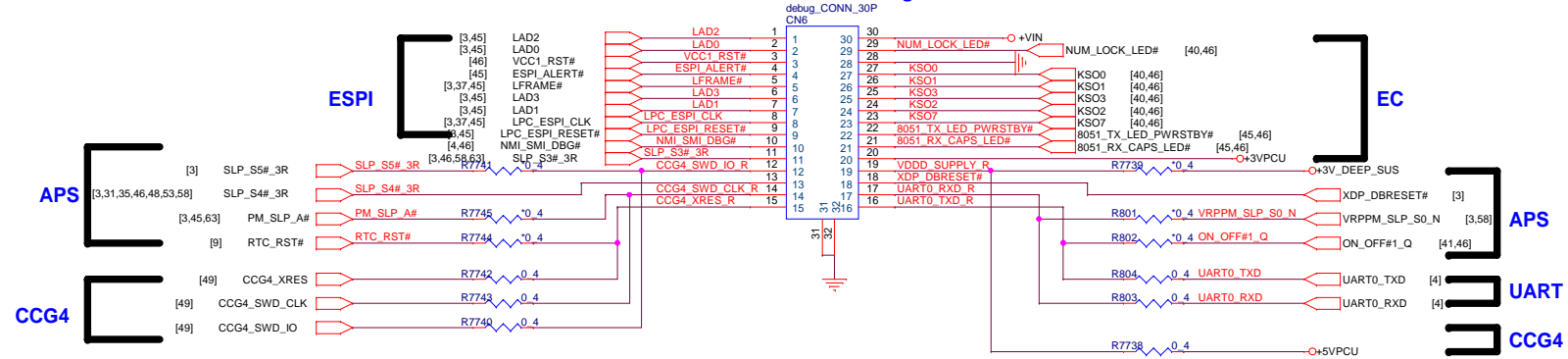
SATA-HDD



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
[8,27,29,30,40,42,54,58,63]

+3V
+5V

ESPI+EC+APS debug conn on MB

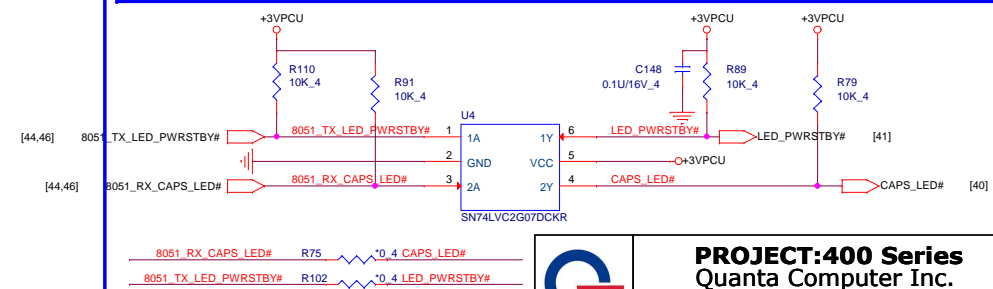
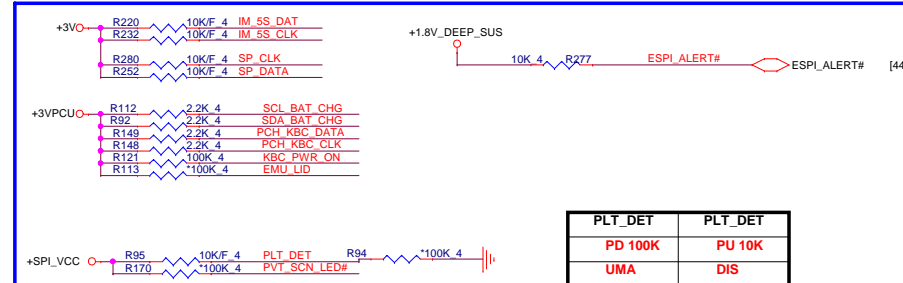
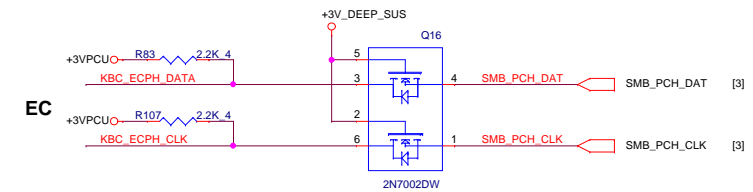
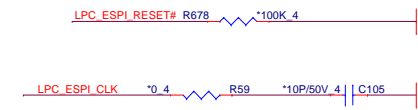
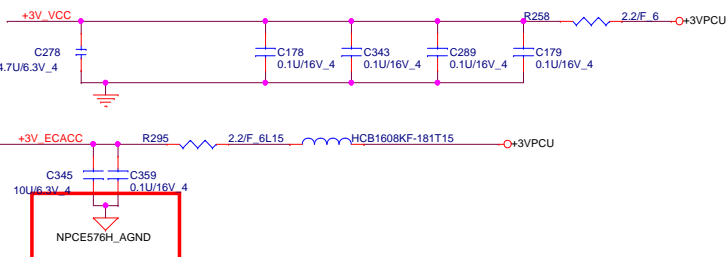
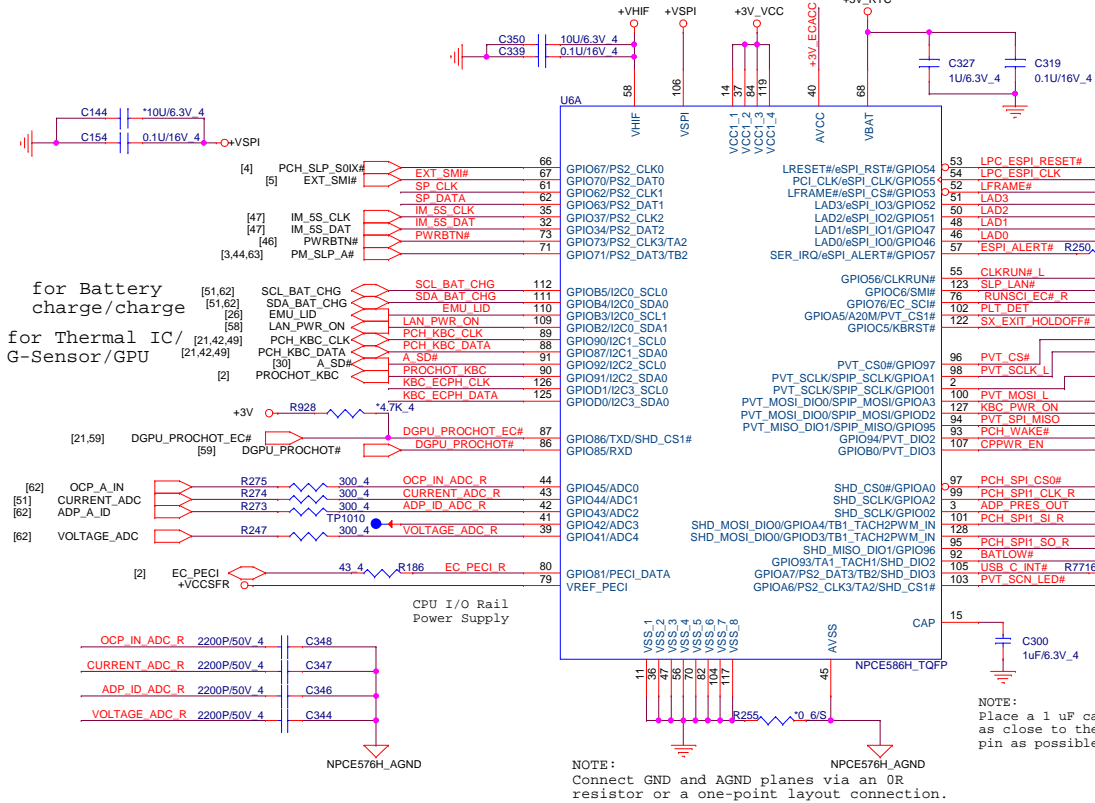


LPC & ESPI TABLE

	LPC MODE	ESPI MODE
R771	INSTAL	UNINSTAL
R769	UNINSTAL	INSTAL
R770	INSTAL	UNINSTAL

LPC & ESPI TABLE

	LPC MODE	ESPI MODE
R658	Ra INSTAL	UNINSTAL
R646	Rb INSTAL	UNINSTAL
R659	Rc INSTAL	UNINSTAL
R656	Rd INSTAL	UNINSTAL
R649	Re INSTAL	UNINSTAL
R657	Rf INSTAL	UNINSTAL
R249	Rg INSTAL	UNINSTAL
R147	Rh INSTAL	UNINSTAL
R120	Ri INSTAL	UNINSTAL
R276	Rj INSTAL	UNINSTAL
R678	Rk UNINSTAL	INSTAL



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,47,51,56,58,59,63]

[9,41,48,51,52,58,62,63]

+3V

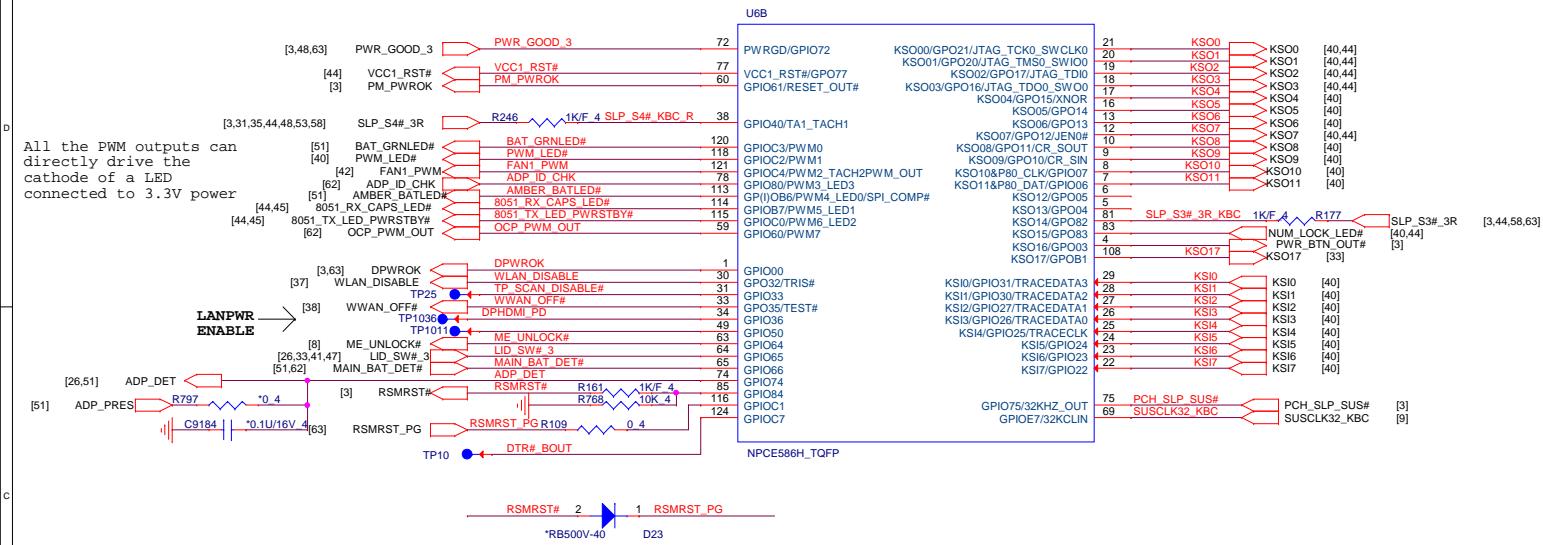
+3V_ALW



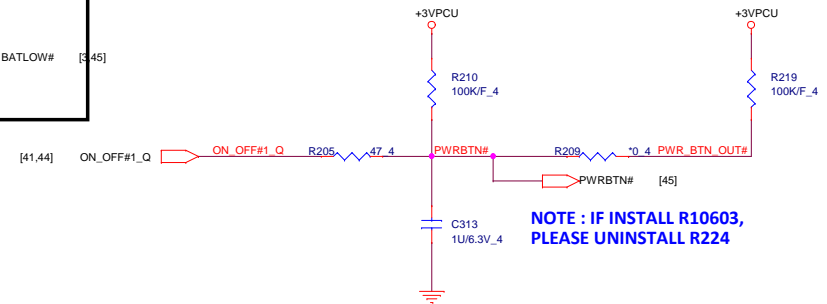
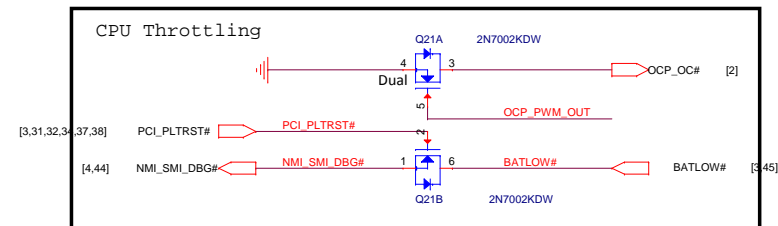
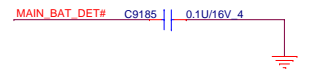
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	45 - EC Nuvoton NPCE586H_1	1A
Date: Thursday, May 12, 2016	Sheet 45 of 65	

All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power

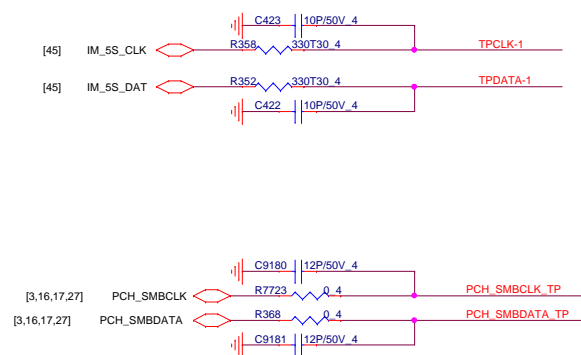
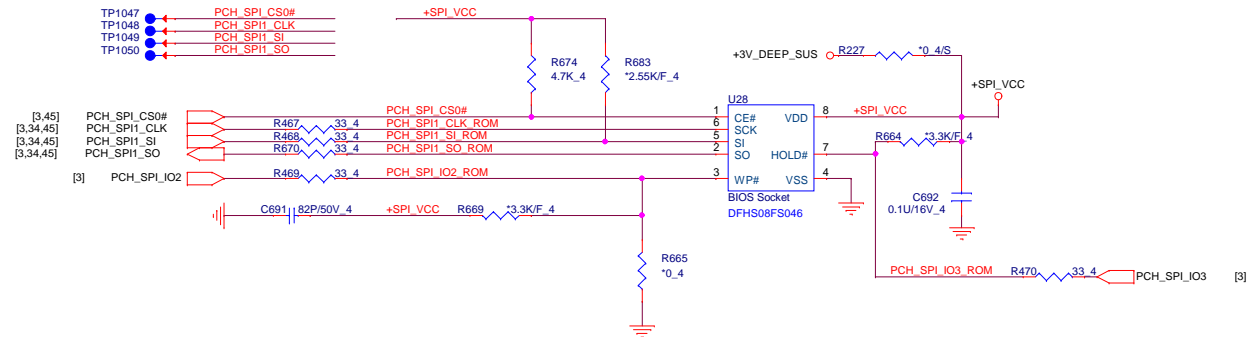


ESD SOLUTION



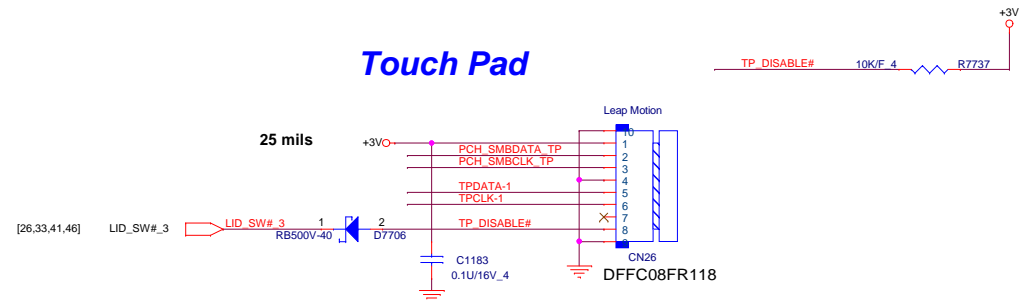
Vender	Size	P/N
GD	128MB	AKE2DF0KQ00
Winbond	128MB	AKE3DZKNK00
Socket		DFHS08FS046

PCH SPI ROM(CLG)

PCH 6*5mm WSON 16M
SPI ROM Socket

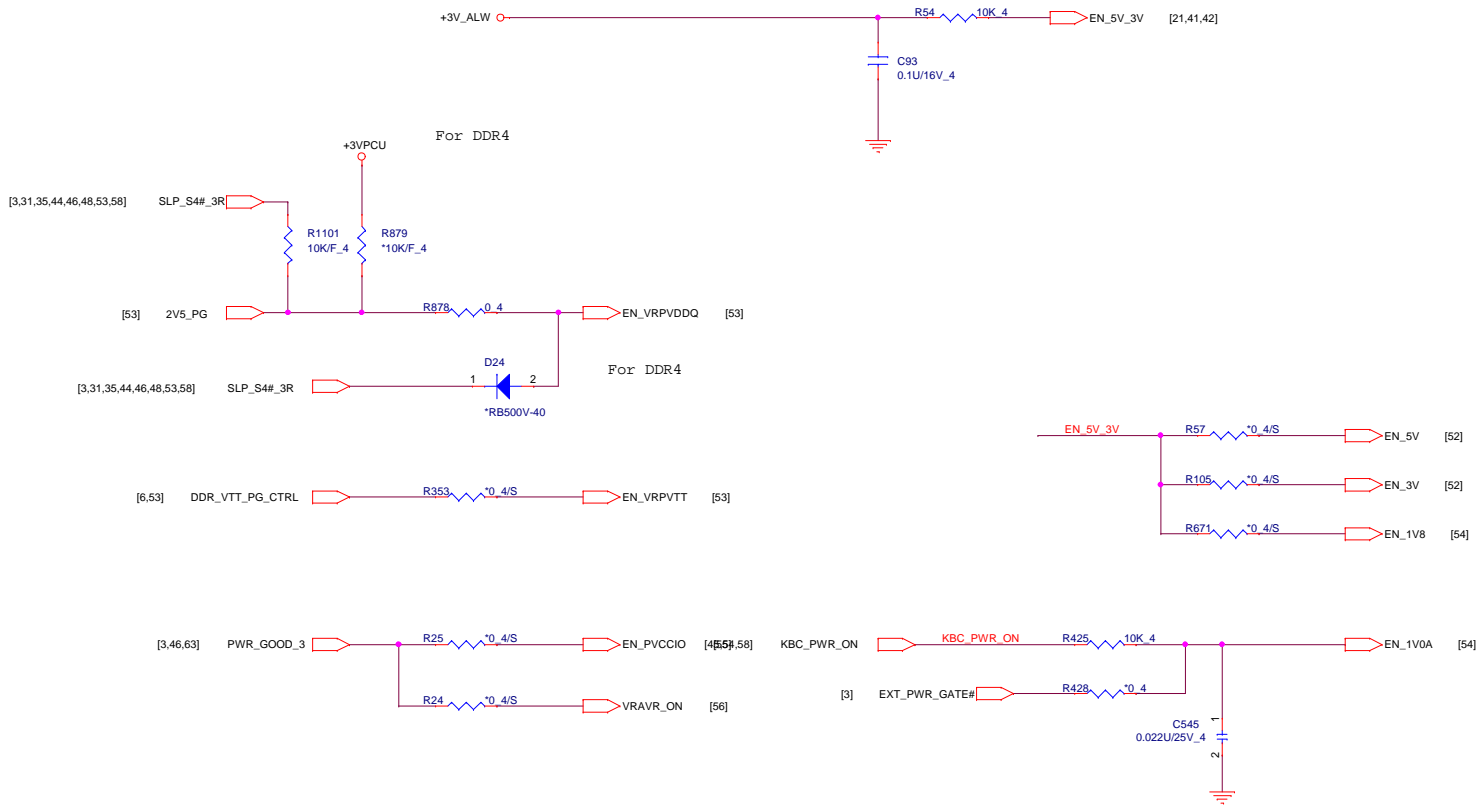
CLICK PAD
Address: 0x20(7 bit)

Touch Pad

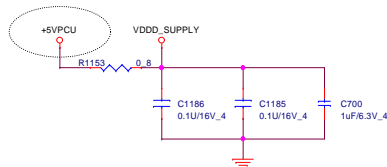


400 series 1001

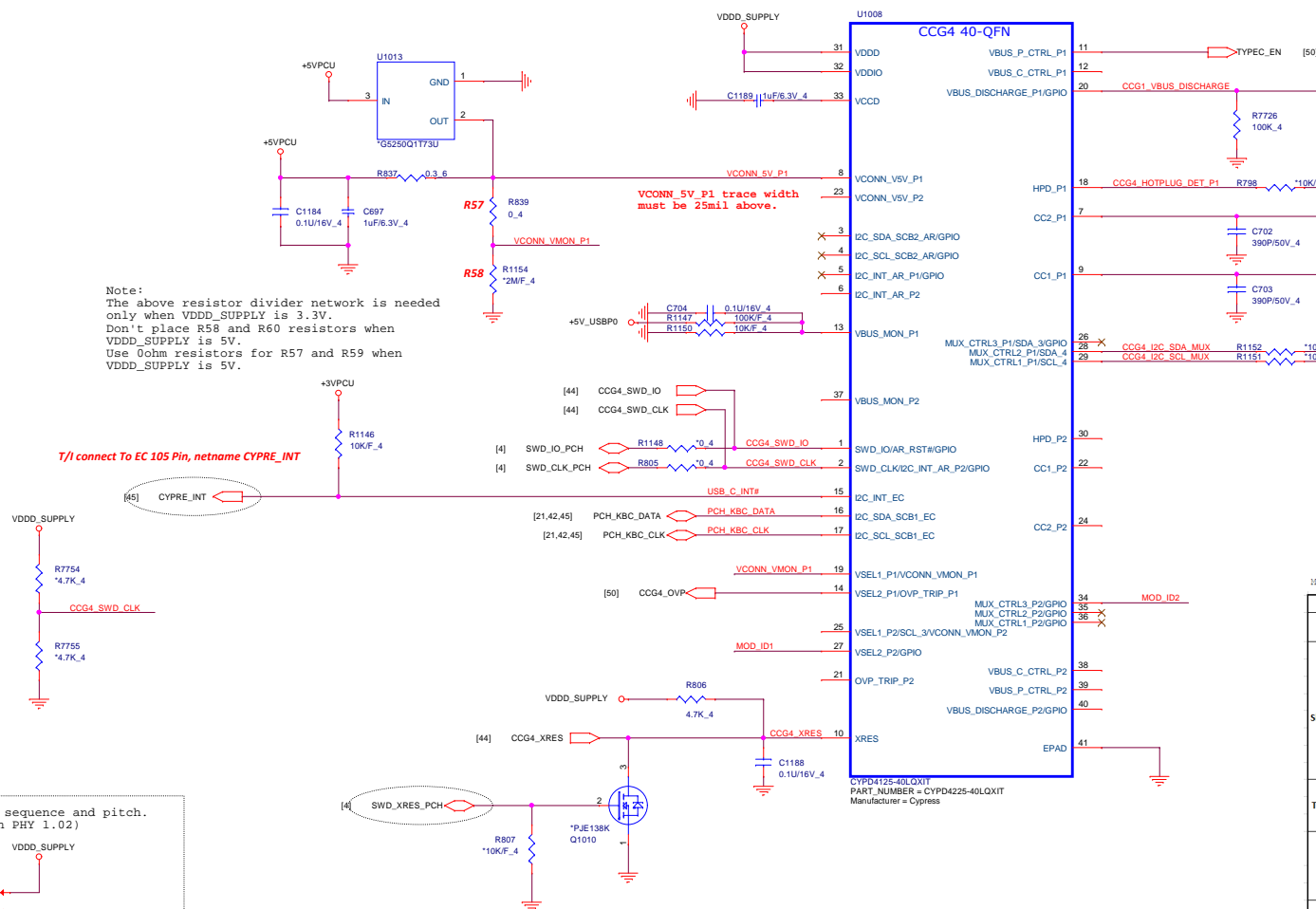
POWER TO EE NET NAME CONNECTION



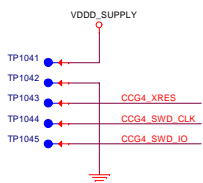
SI, 2/22, Change 5V



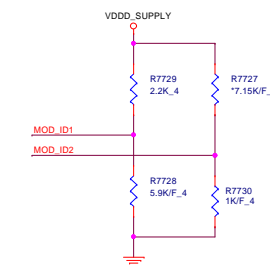
Note:
The above resistor divider network is needed only when VDD_{SUPPLY} is 3.3V.
Don't place R58 and R60 resistors when VDD_{SUPPLY} is 5V.
Use 0ohm resistors for R57 and R59 when VDD_{SUPPLY} is 5V.



test points sequence and pitch.
(2.54mm with PHY 1.02)



MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L5	3.09K	5.1K
L6	2.2K	5.9K



MOD ID1 and MOD ID2 pins connect to ADC in CCG4


	Platform ID		Dual Port	Single Port			
	MOD_ID1	MOD_ID2	Description (Dual port)	Dual Port CFGBID	Description (Single)		Single Port CFGBID
Non TBT Slice Modules	L7	L0	Discrete GFX module for Slice	CFG0			L0 = 0V
	L7	L1	HDD module for Slice	CFG1			L1 = VDDO/3
	L7	L2	ODD module for Slice	CFG1			L2 = 2* VDDO/
	L7	L3	Legacy I/O module for Slice	CFG1			L3 = 3* VDDN/
	L7	L4			Communication	CFG0	L4 = 4* VDDO/
	L7	L5	Future use				L5 = 5* VDDO/
	L7	L6	Future use				L6 = 6* VDDO/
TBT platforms	L7	L7	Future use				L7 = 7* VDDO/
	L0	x	TBT Module for Slice	CFG2			
	L1	x			Slice Gen2	CFG1	
	L2	x			800 & 600, AIO Add-on Card	CFG2	
Non TBT Desktop Platforms	L5	L0	Slice Gen1 & Gen2	CFG3	Slice Gen1	CFG3	
	L5	L1	800 & 600 Series	CFG4	800 & 600, 400 Series (DFP)	CFG4	
	L5	L2	Future		800 & 600 (DFP+DP)	CFG5	
Non TBT Notebook Platforms	L6	L0	DRP I/O on two ports	CFG5	DFP only	CFG4	
	L6	L1			DFP + DP on single port	CFG5	

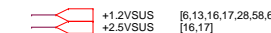


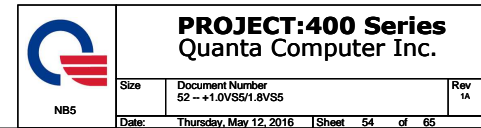
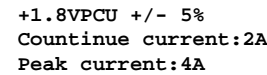
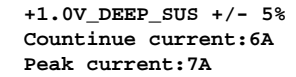
PROJECT:400 Series
Quanta Computer Inc.

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	49 -- Cypress CCG1	1
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 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size	Document Number 50 ~ 35V55 (SY8208B/SY8208C)	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 52 of 65	

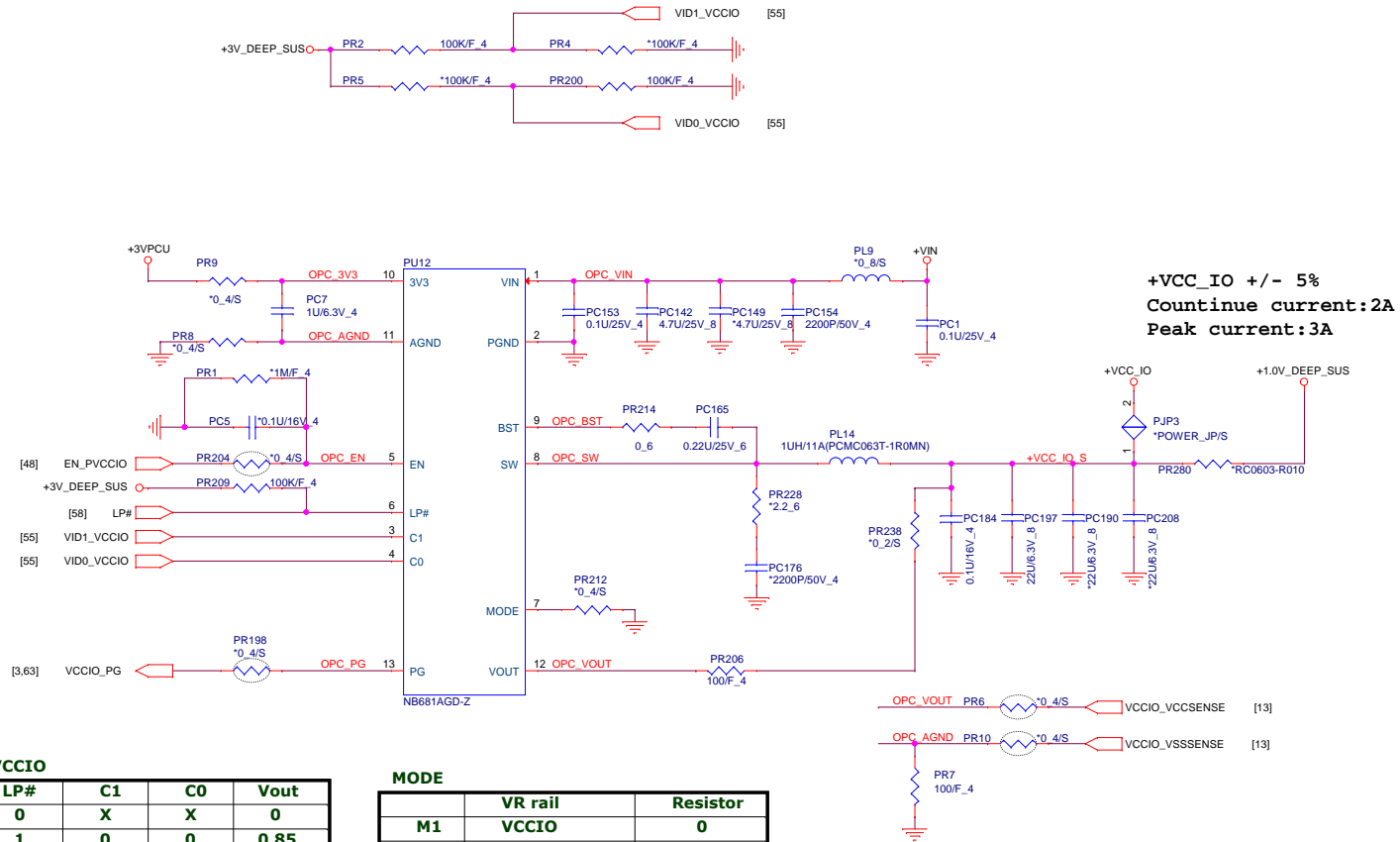




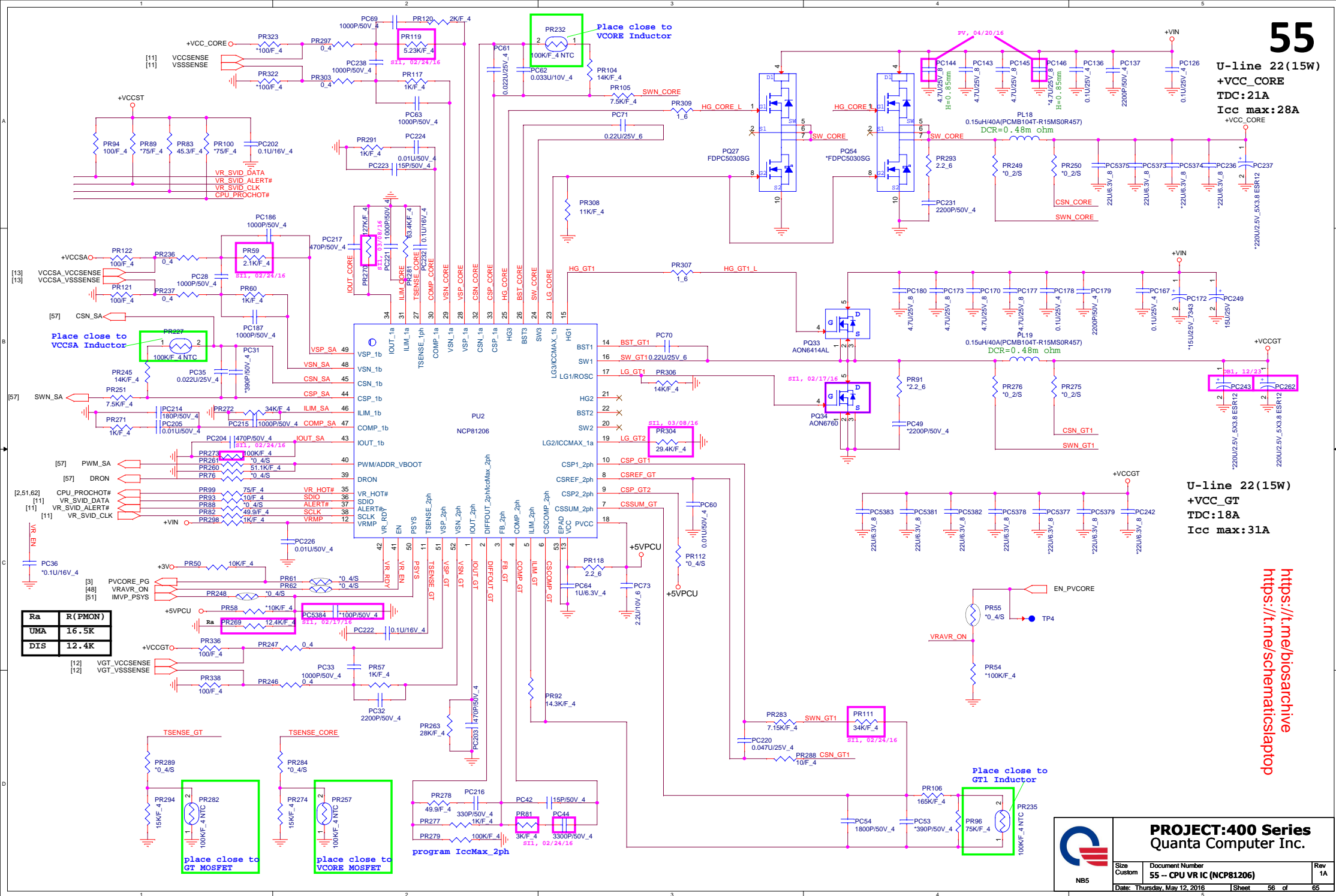
https://t.me/biosarchive
https://t.me/schematicslaptop

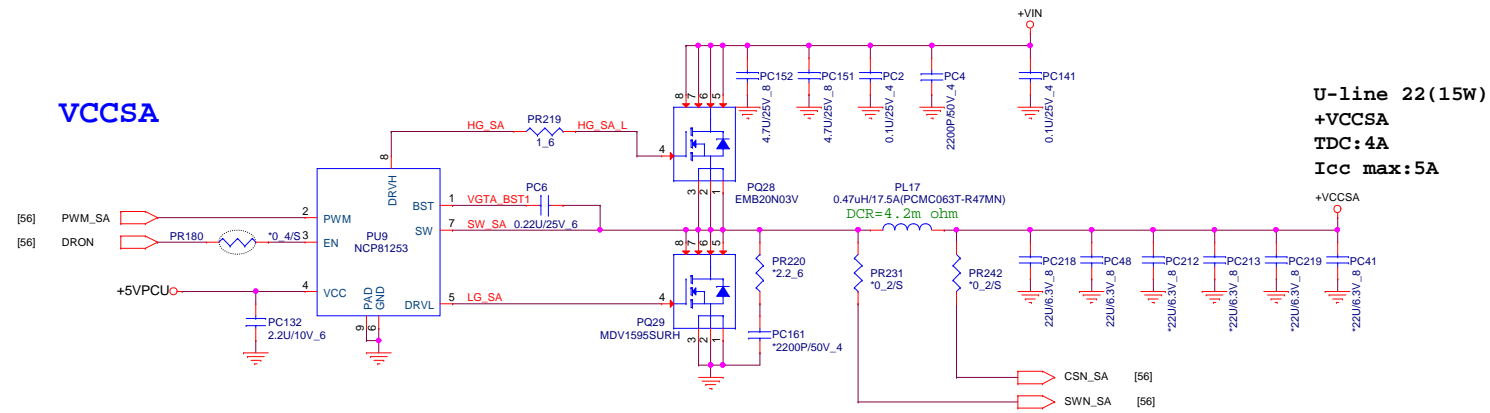
[26,28,44,51,52,53,54,56,57,58,59,61,66]
[9,41,48,51,52,58,62,63]
[5,13]

+VIN
+3V_ALW
+VCC_IO



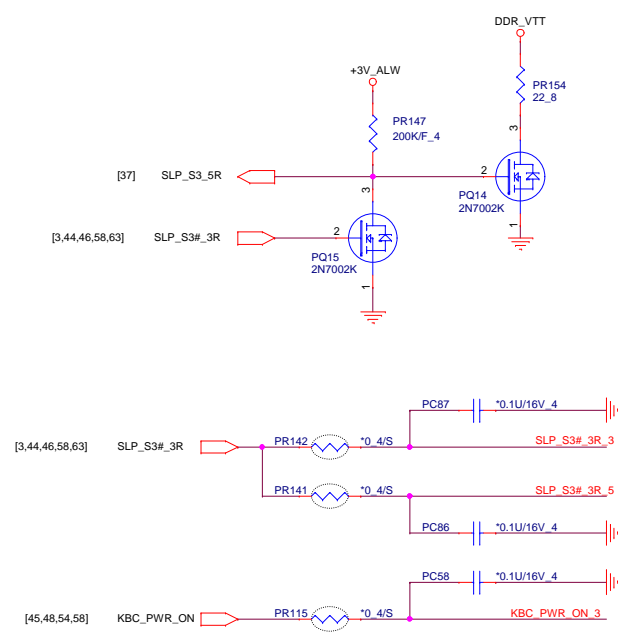
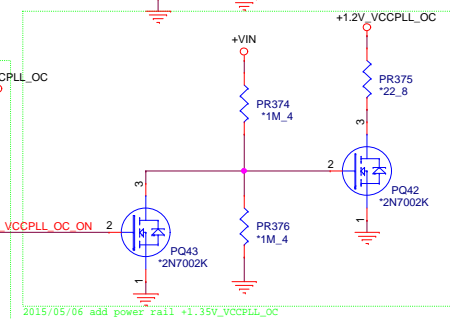
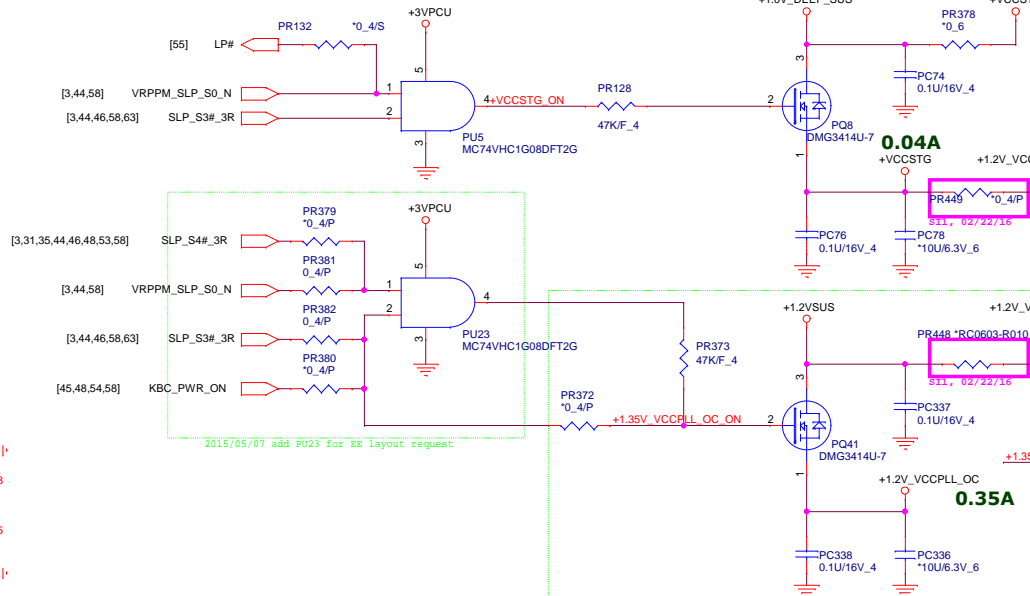
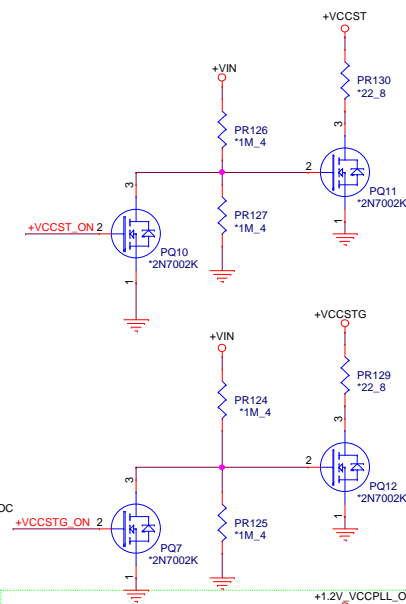
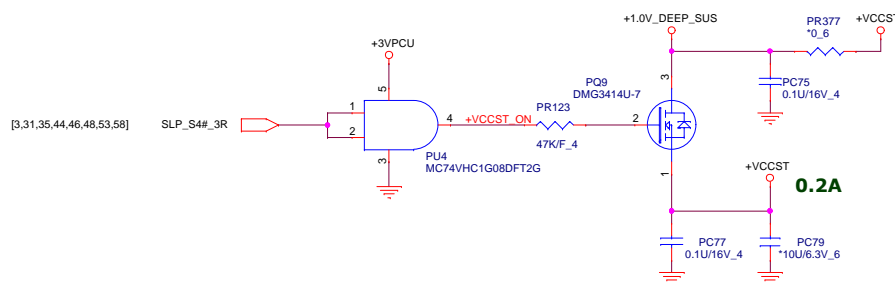
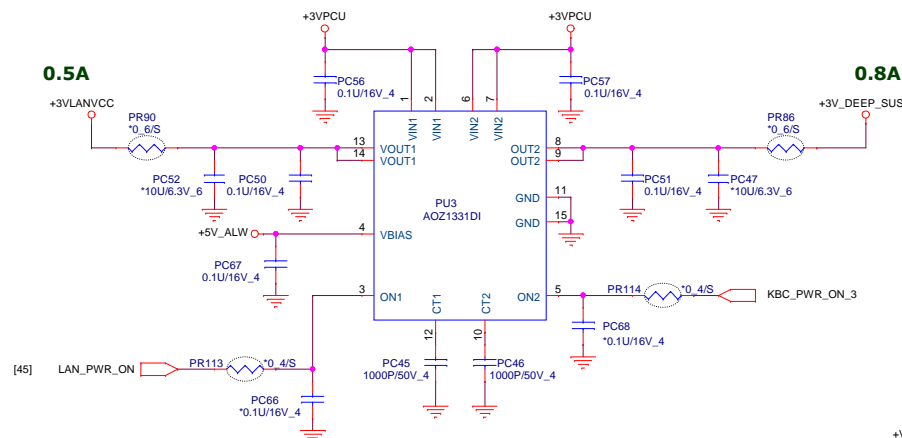
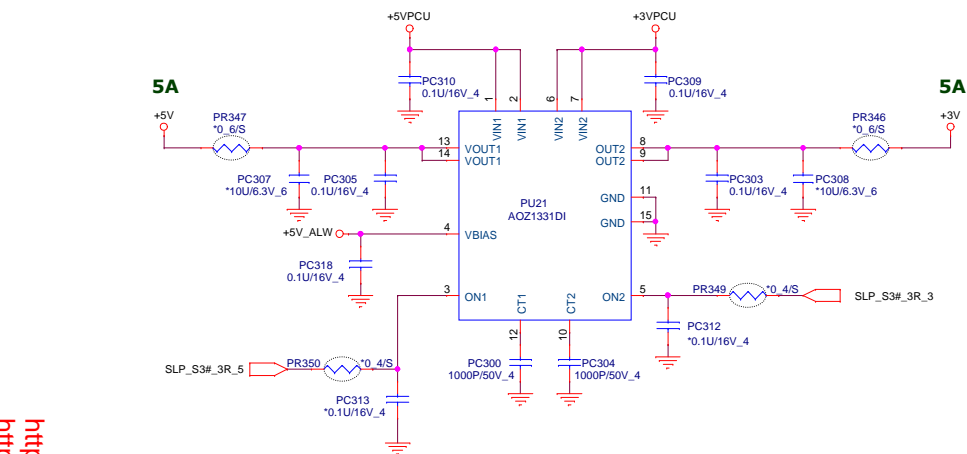
U-line 22(15W)
+VCC_CORE
TDC:21A
Icc max:28A

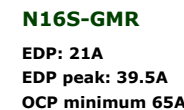


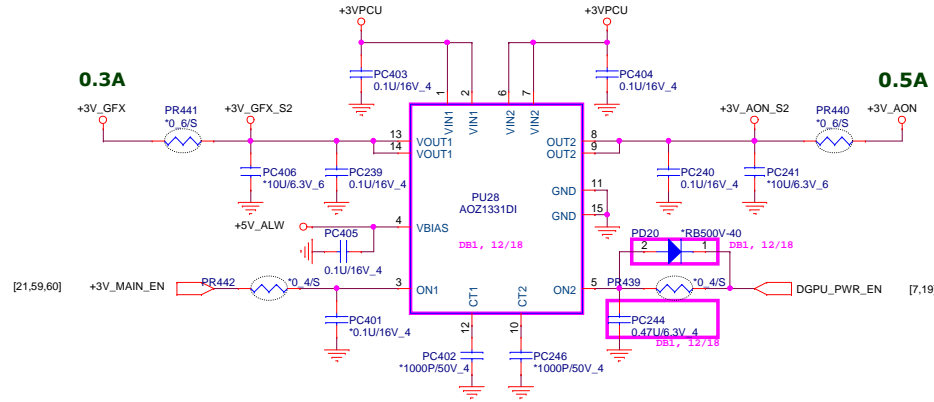


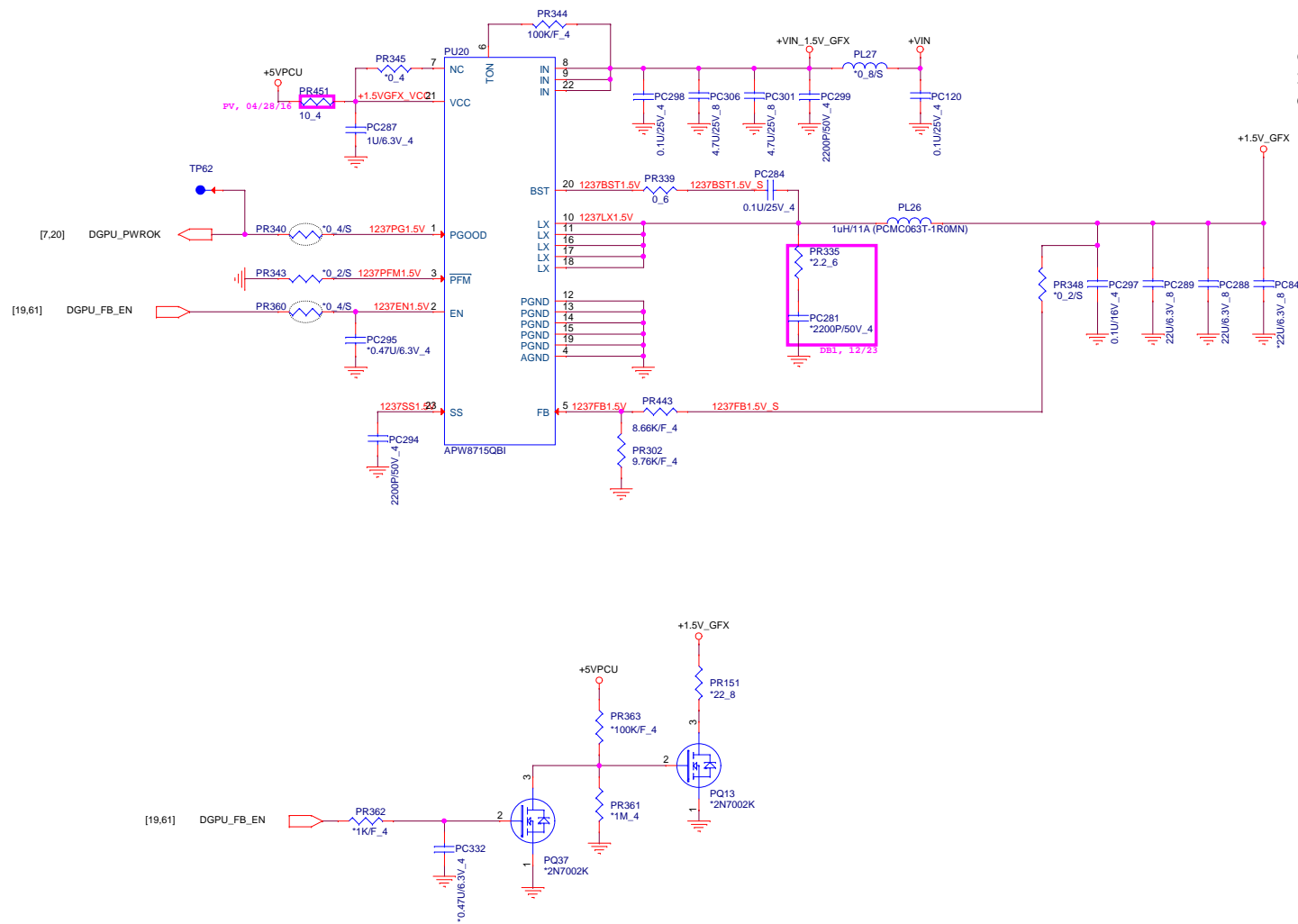
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<https://t.me/schematics4laptop>

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<https://t.me/schematics4laptop>









```
+1.5V_GFX Volt +/- 5%
Countinue current:2.4A
Peak current:4.1A
OCP minimum:8A
```

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POK CKT

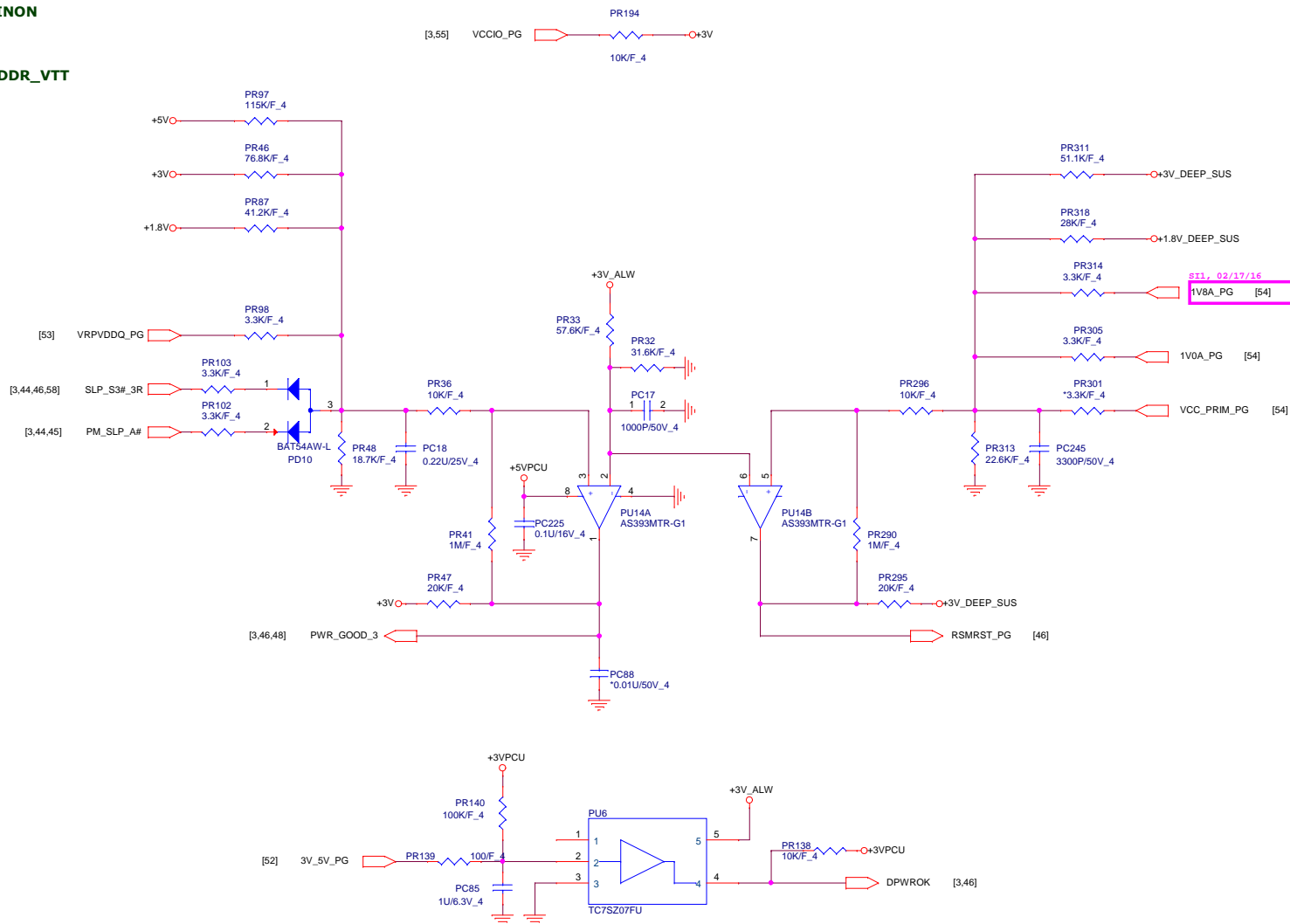
PM_SLP_S4# = SUSON

PM_SLP_S3# = MAINON

+V5S = +5V

+V3S = +3V

+V0.75S = +0.75V_DDR_VTT



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59]

[8,27,29,30,40,42,43,54,58]

[9,41,48,51,52,58,62]

+3V

+5V

+3V_ALW



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Quanta Computer Inc.

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Custom	63 - PWROK	1A
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SKYLAKE U

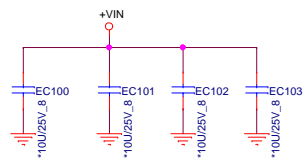
EC
NPCE586H

<https://t.me/biosarchive>
<https://t.me/schematics4laptop>

Example: *499/F_4 and *0_6/S
* means none-installed
499 means value
F means 1%
_4 means 0402 size
/S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC



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